A Tunable and Reduced Size Power Divider Using Ferroelectric Thin-Film Varactors

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***Abstract*— A new concept for a reduced size and tunable power divider is presented based on Barium-Strontium-Titanate (BST) varactors. The proposed topology operates like a conventional Wilkinson power divider while achieving size reduction and a frequency agile behavior in the frequency range of 1.7 GHz to 2.1 GHz. Tuning the operating frequency is achieved by substituting the quarter-wavelength transmission line segments with equivalent lowpass structures and using ferroelectric varactors as tuning elements. A prototype circuit was implemented and characterized showing good agreement between simulation results and measurements. The additional insertion loss in both output branches varied from 1.2 dB to 0.6 dB while maintaining a worst case amplitude- and phase difference of 0.5 dB and 9 degrees respectively for all operating cases. The isolation between the two output ports exceeded 25 dB over the whole tuning range.**

I. Introduction

The continuously rising number of communication standards, which have to be covered by modern mobile radios, calls for reconfigurable and frequency agile front-end components. Already known techniques of designing microwave systems can be adapted in order to incorporate new functionalities, e.g. tunability and thus enable new system architectures with reduced number of functional blocks. Tunable passive components, like ferroelectric varactors, have introduced a whole new group of tunable subsystems, e.g. filters [1], phase shifters [2], and matching networks [3]. In this paper a new approach for the Wilkinson power divider [4] is presented which achieves both, size reduction and a tuning function. The operating principle is based on already known techniques but is enhanced with a new functionality introducing the ferroelectric varactors. The familiar power divider performance is obtained for different operating frequencies and thus enable the circuit to operate as a frequency agile solution. Designing high performance circuits based on tunable components is a challenging task and is mainly influenced by the structure of the component, the electrical behavior, and also its assembly within the circuit. Therefore all of these aspects are discussed in the following sections. In section II the used ferroelectric varactors and their electrical performance is presented, while in section III the proposed power divider topology is discussed. Finally, in section IV the implemented prototype circuit and the corresponding measurement results are shown.

II. Ferroelectric Varactors

The used tunable passive components are BST thin-film varactors where the ferroelectric film is located between the two metal electrodes and together they form the parallel plate capacitor. An electrical field $\vec{E}$ is built by applying a bias voltage V on the electrodes, which are separated by the thin-film of height d. This field, which is straight forward related to the bias voltage as V/d, alters the permittivity of the BST-film and can be described in a mathematical manner [5]. The

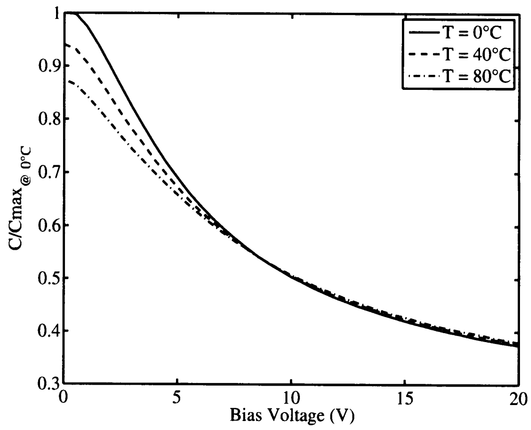

Fig. 1. Normalised on-wafer measured capacitance of a 5 pF varactor for different temperature conditions.

voltage dependence of the BST-varactors is shown in Fig. 1 for a 5 pF capacitor. The measurements were taken with an Agilent E4991A RF-impedance analyzer for frequencies up to 3 GHz by an on-wafer procedure and after the appropriate SOL (Short Open Load) [6] calibration. The capacitance value C as well as the varactor quality factor Q were extracted from the measured input admittance Y according to Eqs. (1) and (2), respectively.

$$C = \frac{\Im\{Y\}}{2\pi f} \quad (1)$$

$$Q = \frac{\Im\{Y\}}{\Re\{Y\}} \quad (2)$$

The maximum capacitance is decreasing for higher temperatures, as predicted by the Ginzburg-Landau theory [7], since

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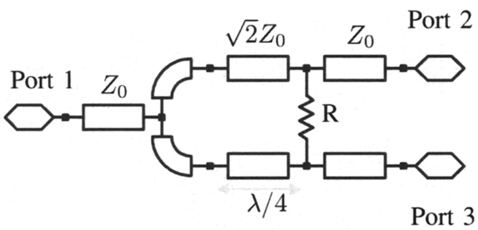
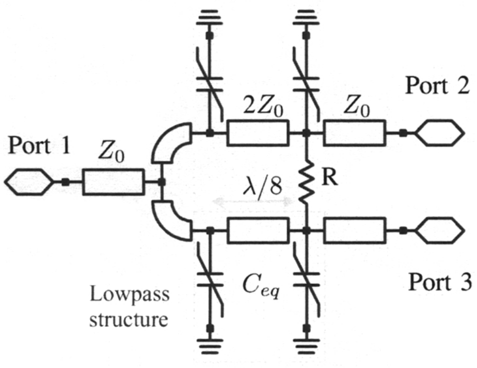
the operating temperature in the crystal moves far away from the phase transition point. Therefore the achievable relative permitivity ϵ_r decreases and thus the obtained maximum capacitance, since $C=\epsilon_r\epsilon_0 A/d$ where A is the effective electrode area. For high temperatures the maximum measured capacitance, which is always obtained at zero bias, decreases more than 10%. At low temperatures a tunability of more than 60% is achievable at a bias voltage of 20 V. The measurements showed quality factor values Q higher than 40 in the frequency region from 1.7 GHz to 2.1 GHz. The overall electrical behavior of BST thin-film varactors can be described by equivalent models [8], thus allowing accurate linear and nonlinear simulations during the design procedure.

III. Wilkinson Divider Design

The power divider proposed by Wilkinson is based on quarter-wavelength transmission line segments and is presented in Fig. 2(a). The input and output port impedances are Z_0 while the $\lambda/4$ segments have an impedance of $\sqrt{2}Z_0$. The



(a) Wilkinson divider



(b) Reduced size power divider

Fig. 2. Power divider topologies.

output branches are connected through a resistor with $R=2Z_0$ thus enabling impedance matching at all ports and isolation between them at the $\lambda/4$ resonance frequency. The reduced size topology presented in Fig. 2(b) uses the principle of substituting the $\lambda/4$ segments with equivalent lowpass structures [9]. The new transmission line segments have a shorter electrical length and a higher impedance. Lumped capacitors are used in order to compensate for the shorter propagation path. The $\lambda/4$ transmission line segment of impedance $\sqrt{2}Z_0$ can be substituted by an equivalent segment of length $\lambda/8$ with an impedance of $2Z_0$ by adding two lumped capacitors

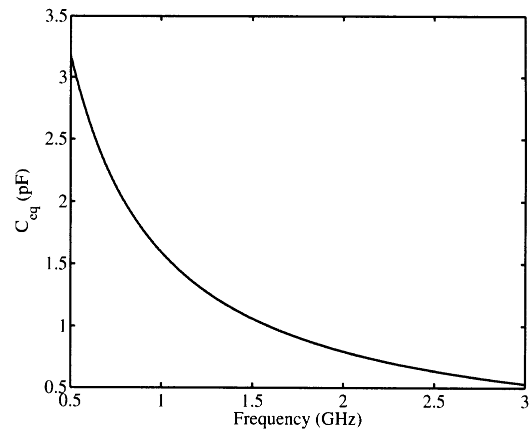


Fig. 3. Resulting capacitor value C_{eq} for substituting a $\lambda/4$ transmission line segment of impedance $\sqrt{2}Z_0$ with a $\lambda/8$ transmission line segment of impedance $2Z_0$, where Z_0=50 Ω.

to the transmission line, with a capacitance value of

$$C_{eq} = \frac{\cos(\pi/4)}{\omega\sqrt{2}Z_0} = \frac{1}{4\pi f Z_0}. \qquad (3)$$

Here ω and f denote the angular and operating frequency respectively. The design methodology is fully scalable for different frequencies and impedances since it is based on transformations with closed formulas. Possible limitations could arise only due to manufacture tolerances of the resulting impedance levels for the transmission lines.

The resulting capacitor value C_{eq} for the targeted frequency region is depicted in Fig. 3. It is evident from this diagram, that the resonance frequency of the equivalent quarter-wavelength line structure is shifted by altering the capacitor value C_{eq}. Thus by using tunable capacitors, e.g. BST-varactors, a tuning functionality is added to the topology. Increasing the bias voltage would result in lowering the varactor capacitance and thus shifting the equivalent $\lambda/4$ resonance toward higher frequencies. The only penalty is inserting some additional components in order to supply the bias voltage and avoid DC current flow over the input and output ports. The targeted operating frequency region was 1.7 GHz to 2.1 GHz in order to serve as a frequency agile power divider solution for mobile applications. Therefore varactors with C=1 pF were selected. The original power divider performance is retained since the topology is still symmetrical.

IV. Prototype implementation and measurements

A prototype board of the proposed power divider circuit was implemented on a Rogers RO3010 substrate with height h=1.27 mm and dielectric constant ϵ_r=10.2. The fabricated board, including feeding lines, has an area of 35 mm × 35 mm and the circuit trace is depicted in Fig. 4.

The prototype was characterized through S-parameter measurements which were taken with a Rohde & Schwarz ZVB8 vector network analyzer after the appropriate SOLT (Short Open Load Through) calibration. The BST-varactors were

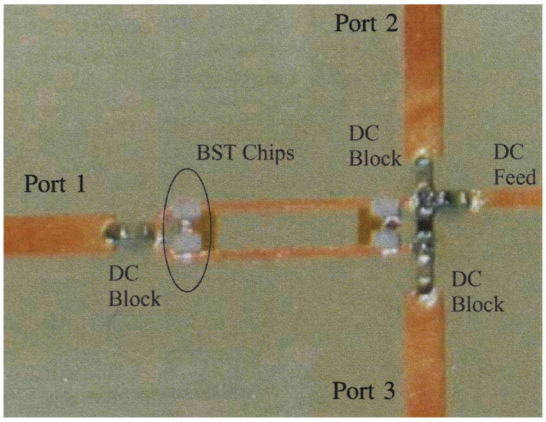


Fig. 4. Fabricated prototype board of the proposed tunable power divider.

assembled in a flip-chip procedure in order to eliminate the resulting parasitic wire inductance and the associated loss mechanisms of conventional ball-wedge or wedge-wedge wire assemblies. These interconnection parasitics are especially troublesome for higher operating frequencies and broadband applications since the feeding wire inductance causes a rapidly rising effective capacitance. Gold stud bumps were placed on the varactor chip pads and connected to the metal traces of the board via a conductive adhesive. These interconnects can be described by equivalent lumped element models [10] and thus incorporated into the design procedure.

For the design Agilent's Advanced Design System (ADS) was used. Good agreement was obtained between simulation results and measurements as illustrated in Fig. 5.

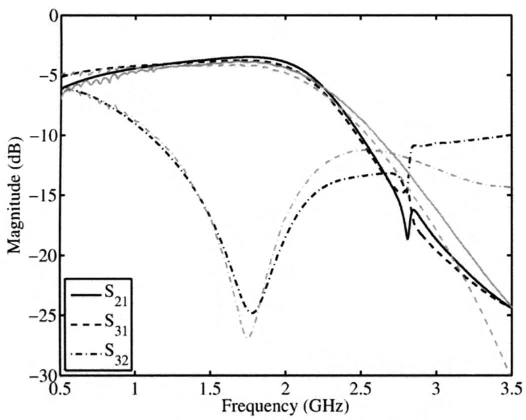


Fig. 5. Measured (grey) and simulated (black) transmission and isolation S-parameters.

The input port matching parameter is shown in Fig. 6, whereas in Fig. 7 the corresponding isolation between the two output ports is presented. The provided power at port 1 is divided equally between the two output ports for all operating bias states as can be seen in Fig. 8 and the amplitude difference remains below 0.5 dB, within the targeted communication

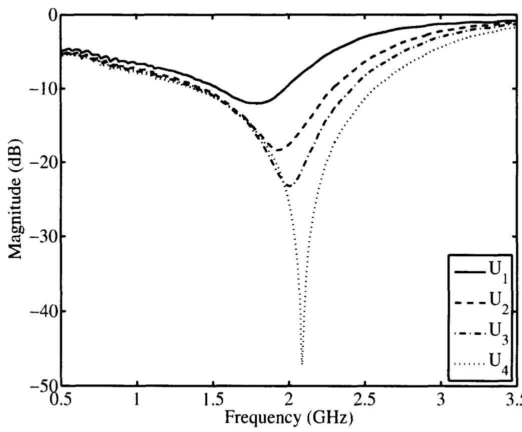


Fig. 6. Measured input matching S-parameter S_{11} for different bias states U_1 – U_4.

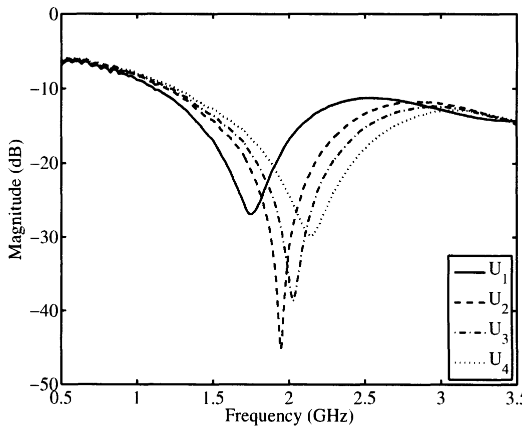


Fig. 7. Measured output isolation S-parameter S_{32} for different bias states U_1 – U_4.

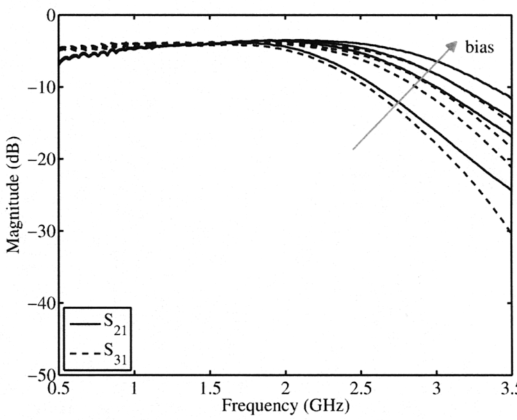


Fig. 8. Measured transmission S-parameters S_{21} and S_{31} for different bias states U_1 – U_4.

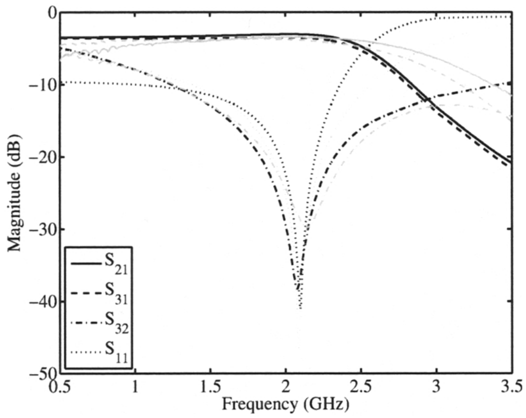


Fig. 9. Measured S-parameters (grey) of the prototype circuit and simulated data (black) for the same reduced size power divider with Murata-GJM15 SMD capacitors.

bands. The additional insertion loss varies from 1.2 dB to 0.6 dB depending on the applied bias state and the worst case phase difference is 9 degrees, which is mainly due to varactor value tolerances. The transmission curves reveal the inherent lowpass characteristic of the circuit which is beneficial in terms of linearity performance since higher order harmonics are suppressed better than by a conventional power divider topology.

A comparison between the measured S-parameters of the tunable circuit with BST-varactors and simulated data for the same topology with high-Q SMD capacitors is presented in Fig. 9. The prototype circuit shows a similar narrow band performance in the targeted frequency region and a slightly higher insertion loss. Nevertheless, tuning the resonance frequency results in noticeable performance enhancement for the other frequency bands as demonstrated previously.

V. Conclusions

A novel design approach for a tunable and size reduced power divider is presented based on ferroelectric thin-film varactors. The design methodology is fully scalable for different impedances and frequency regions. The circuit performance showed good agreement to the simulated data and the operating frequency band can be tuned continuously from 1.7 GHz to 2.1 GHz thus allowing multi band operation for mobile applications. While the narrow band behavior of the original Wilkinson divider topology is retained an improved isolation between the two output ports is achieved over a broad frequency region. The used topology exhibits size reduction and a tuning function while showing an additional lowpass characteristic in the two transmission paths. Symmetrical power splitting is achieved, in both amplitude and phase, between the output ports and thus fulfilling the divider operation.

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