EDA Toolsets for RF Design & Modeling

Yiannis Moisiadis, Errikos Lourandakis, Sotiris Bantas

Helic, Inc. 101 Montgomery str., suite 1950 San Fransisco, CA 94104, USA

Email: {moisiad, lourandakis, s.bantas}@helic.com

Abstract

This paper presents two powerful EDA toolsets, which enable fast and accurate modeling of inductors, RF interconnect lines and bondwires. The modeling methodology is based on a set of algorithms derived from EM theory and is orders of magnitude faster than any generic EM solver. The following tools will be discussed: VeloceRF™, which enables fast synthesis and optimization of DRC and DFM clean RF components, such as spirals, transformers and RF interconnects, and supports ultra-fast electromagnetic extraction. VeloceWired™, which enables rapid bonwire synthesis and modeling, within the standard IC design platforms.

This paper describes how these EDA toolsets were put in use to design and fabricate a VCO in TSMC 65nm CMOS technology. Measured results on the VCO, fabricated in TSMC 65nm CMOS technology, prove the accuracy and efficiency of the modeling methodology with first-pass successes.

1. INTRODUCTION

While for commercial transistors the minimum length has been scaled down to 28nm, passive component parasitics are not scaling with the minimum transistor feature size. As a result, improvements in RF circuit performance that can take advantage from scaling continue to be constrained by the passive components surrounding the active devices. This includes on-chip interconnect, inductive components determining the performance of critical blocks, such as the tuning frequency of a VCO or the Noise Figure of an LNA, packaging parasitics (e.g., bondwires), as well as the printed circuit or other subassembly. The high frequency effects associated with the passive components are typically viewed as an added problem that a high frequency circuit designer must take into account. More specifically, the concern over on-chip inductance is primarily due to the lack of a thorough understanding of the related effects and an insufficient sophistication of the tools and methods that are available for designing, optimizing and modeling the inductive part of high frequency and RF integrated circuits.

Commercial electromagnetic (EM) field solvers are widely available and can be used to predict the performance of passive components even on a low-cost desktop system [1]. While these tools provide accurate passive models (based on variations of the MoM (Method of Moments) or Finite Element techniques), the computation times required for simulating complete multi-layered circuits are extremely high (several hours or days depending on the system under test). This very long simulation time can render these tools impractical for many design timetables. Furthermore, EM solvers require prior knowledge of electromagnetic to configure critical modeling parameters such as the boundary conditions or custom local meshing, a lot of effort is needed to import the stack-up profile of a given technology, while it is difficult to integrate them in the IC design flow, in order to support verification capabilities. Empirical technique based on curve fitting for symmetrical inductors has been also reported, but models derived this way cannot be scaled to reflect changes in the inductor's layout or fabrication technology and cannot be implemented into a circuit simulator.

Helic Inc., on the other hand, has developed a modeling methodology [2, 3], based on a set of algorithms derived from EM theory, which can efficiently model complex cross-coupled devices on any silicon substrate. The specific methodology has been adopted for different applications such as inductors synthesis, optimization and modeling (VeloceRF™) and bondwire synthesis and modeling (VeloceWired™). The modeling methodology is orders of magnitude faster than any generic EM solver. This dramatically reduces the design effort and number of silicon and package test runs required to optimize a system. Consequently, this results in going to market much faster, at much lower cost and with a near-optimum design. The speed of the modeler is attributed to the fact that all calculations (inductance, resistance, capacitance, substrate parasitics, and mutual inductances) employ closed-form formulas, allowing for rapid executing even for very large and complex structures. Furthermore time-consuming calculations such as matrix inversions have been avoided completely in the algorithm to make it even faster.

2. EDA toolset main features

The toolset is seamlessly integrated in standard design flows, like the one implemented by Cadence Virtuoso™. The main features of the tools are described below:

2.1. VeloceRF™

VeloceRF™ enables an inductance-aware RF IC design flow that complements other tools and design functions, such as LVS verification, RC extraction, substrate noise analysis, etc. VeloceRF™ consists of the following three major and distinct modules [4]:

Spiral Wizard™ is an extremely fast, constraint-driven spiral inductor synthesis and optimization engine. It can rapidly and efficiently deliver DRC-clean spirals tailored exactly to the designer's requirements in inductance, operating frequency and quality factor. The design process is significantly simplified and accelerated, as it is disentangled from the use of pre-characterized inductor libraries. The Spiral Wizard features on-the-fly layout synthesis, under an extensive set of constraints that make it possible to optimize inductor quality factor, save silicon real estate and minimize surrounding interconnect.

VeloceRaptor™, an inductive component modeling engine, that support RCLk extraction for any arbitrarily – shaped inductor (multi – layer included), transformers, RF interconnects. The L and Q predictions were found to be accurate within 5% after elaborate testing on more than 15 actual processes. Regarding the dynamic range of the models, these can be either broadband or narrowband; typical operating frequencies range from 100 - 200 MHz up to multi – GHz.

VeloceRules™, powerful pattern recognition flow for spiral components that support Layout-vs-Schematic (LVS) verification and integrate seamlessly with parasitics extraction (RCX).

VeloceRF™ provides spiral inductor parametric cells that can be extracted with full connectivity in a single netlist. The resulting netlist includes mutual coupling (k) elements and is generated automatically, without any need for user intervention or back-annotation. In the back-end stages – verification and extraction – VeloceRF works seamlessly with the DRC, LVS and RCX tools. All VeloceRF devices are governed by an extensive set of callbacks that guarantee DRC clean and DFM correct (Design for Manufacturability) PCells. LVS checks for connectivity and compares inductor properties in the layout and schematics.

VeloceRF™ key features are listed below:

- A compact inductor model is available to facilitate time-consuming transient and non-linear analyses.
- Effects associated with the presence of metal fill patterns are accounted.
- Consideration of temperature effects of VeloceRF™ entities.
- Support of poly or metal mesh shields for integrated spirals
- Unrestricted magnetic coupling modeling.
- No parameter fitting against measurement required.
- Both broadband and narrowband models available.
- Corner models based on technology variation available

2.2. VeloceWired™

VeloceWired™ provides rapid bondwire creation and extraction. The modeling engine of VeloceWired™ enables full RLCk extraction of the bondwire interconnects and captures complex electromagnetic effects such as self and mutual inductances, frequency-dependent resistance and capacitive coupling [5]. A wide variety of bondwire profiles (Jedec types and user defined) are supported, allowing the accurate modeling of virtually any type of interconnect (die-package, multi-die, stacked die) [6].

3. DESIGN EXAMPLE

3.1. VCO DESIGN

A VCO is implemented in a 9metal TSMC 65CMOS technology, to operate in a frequency range between 1.472GHz - 1.704GHz at 1.2V and output load 50 Ohm, exhibiting a phase noise better than -110dBc@1MHz. The microphotography of the VCO is illustrated in Figure 1.

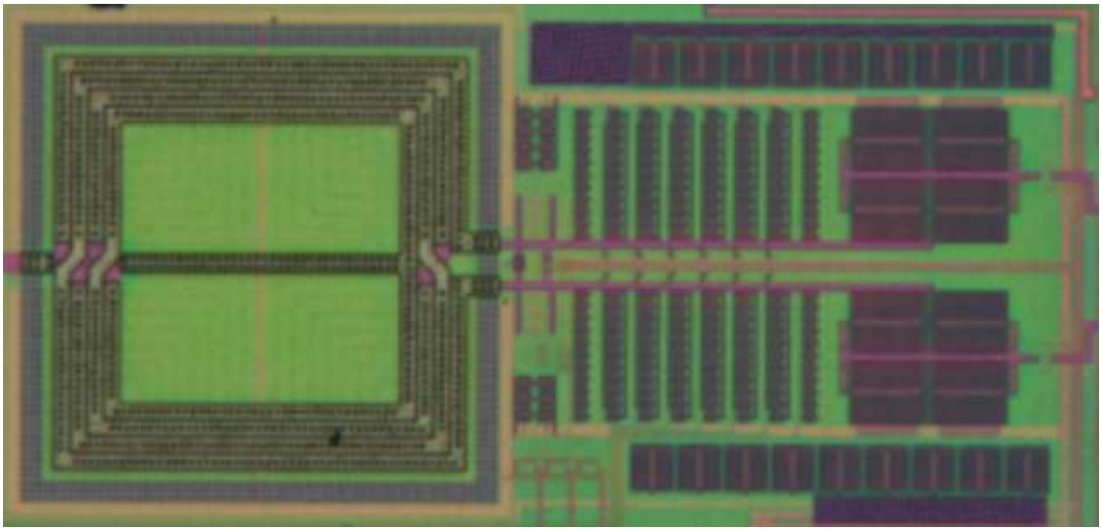

Figure 1: VCO microphotography

The specifications define the choice of core devices in terms of type and size. Between PMOS and NMOS for implementing the negative gm, the choice was PMOS, due to reduced noise. An appropriate MIM capacitor (C), and a pair of varactors (Var1, Var2) properly biased, are placed in parallel to the differential inductor (L), to achieve the desired frequency of oscillation (Figure 2).

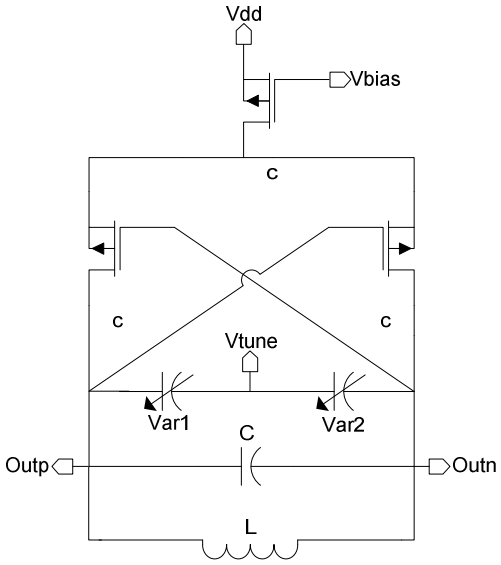

Figure 2: VCO schematic

One of the challenges during VCO design is to support the frequency range for all process variations and temperature corners (-40^{0}C to 110^{0}C). The VCO includes a capacitor array, added in parallel to the VCO resonator, which is digitally controlled through MOS switches. A 6bit capacitor array can sufficiently cover the specified frequency range for all corners. The VCO layout is illustrated in Figure 3.

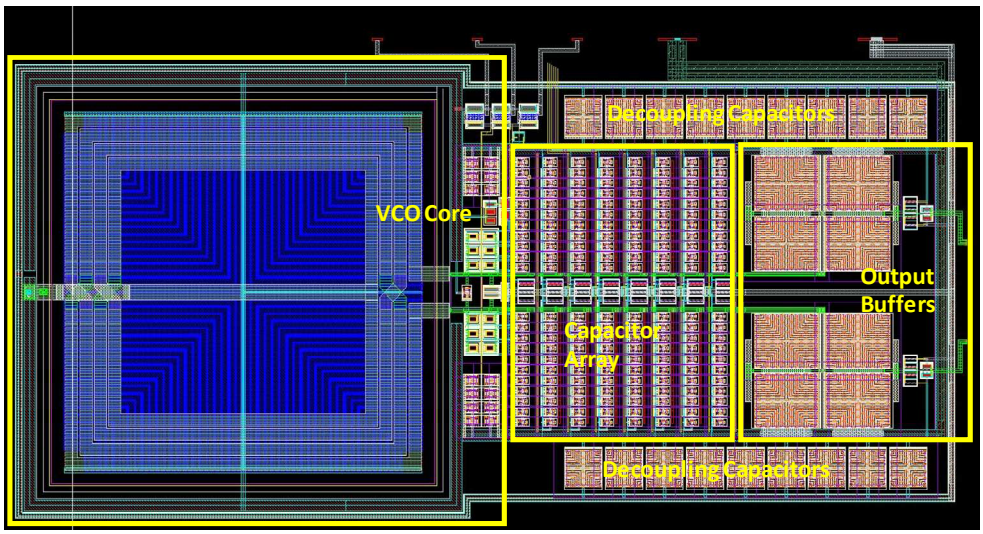

Figure 3: VCO Layout

The quality factor of the VCO inductor directly affects the Phase Noise of the VCO [7]. Having a high-Q value in the frequency of the desired oscillation, helps to achieve phase noise better than -100dbc@1MHz. Using VeloceRF's Spiral Wizard engine an inductor was synthesized that meet the

necessary requirements. For the synthesized inductor, the L and Q curves over frequency are presented in Figure 4. At 1.6GHz, the differential inductor exhibits a Q of 22 and Ldiff of 8.97pH (Figure 4).

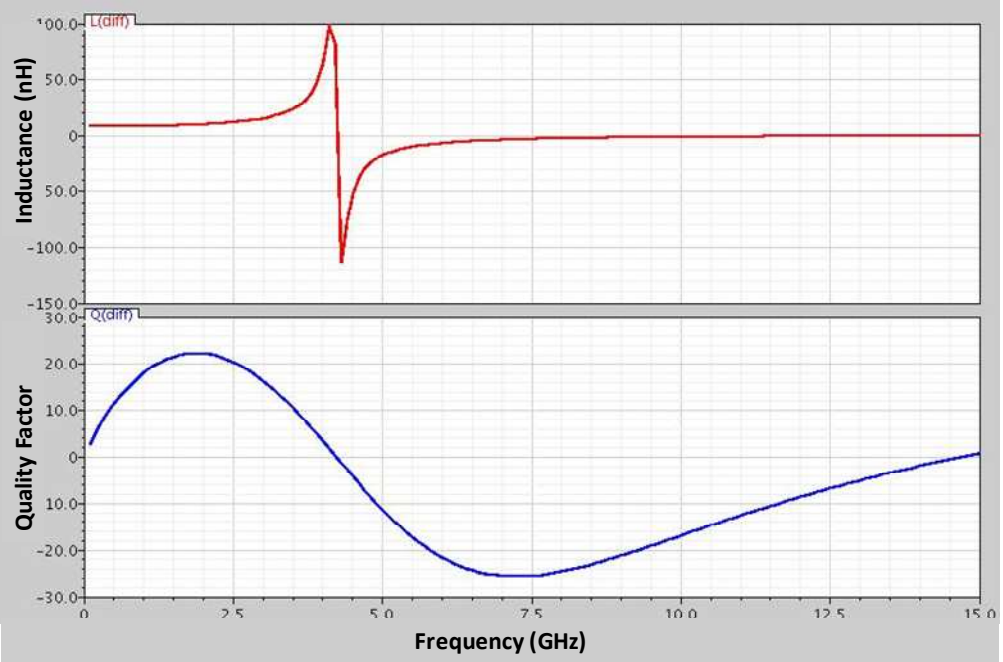

Figure 4: Inductor L, Q characteristics

The inductor value must be properly defined in order to accommodate for the capacitive parasitics of the interconnects, which are expected to lower the frequency of simulation. Though the post-layout simulation takes into account the parasitic capacitances and resistances, it does not take into account the parasitic inductances and mutual coupling. From a simple inspection of the layout it becomes obvious that the connecting metal paths of the differential inductor can seriously affect its performance as they insert a considerable series inductance.

VeloceRF™ provides the Path-to-Inductor option, through which any arbitrary selected path can be converted into an inductive elements (PathInductor) recognized by VeloceRF's modeling engine. By selecting the two paths and converting them to PathInductors, (Figure 5), the VeloceRF model includes RLCk model for the inductor, these two paths and the inductive coupling amongst them. The VCO performance can be further investigated, by taking into account the two parasitic inductances along with their mutual coupling with the rest of the inductive components of the circuit.

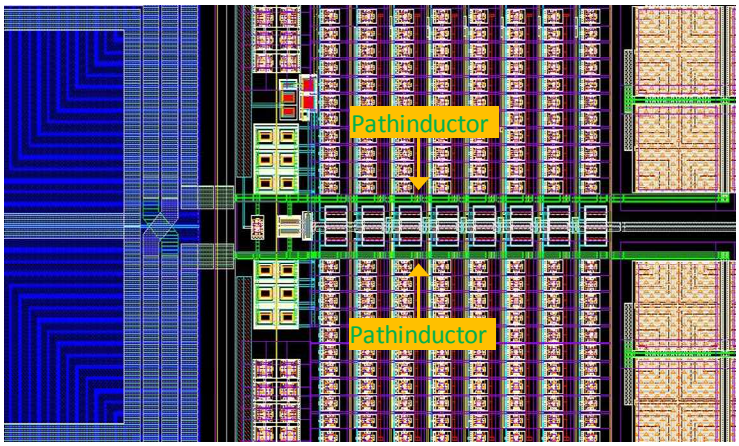

Figure 5: The pathinductors

The die, which includes the VCO, has a size 2mm x 4mm and is packaged in a 56 lead, 8mmX8mm QFN package. Figure 6 presents the bondwires which connect the VCO pads to the QFN package. The bondwires have been designed and modeled with VeloceWired™. The geometry of the bondwires is Jedec-4, with diameter 25um. According to the length of the bondwires, the inductance that is introduced range from 1.8nH to 2.5nH.

Due to the output buffers, the bondwires are not expected to affect the oscillation frequency and phase noise performance. However, they have an impact on the output signal amplitude and introduces phase mismatch between the VCO outputs. Consequently, accurate bondwire modelling will eliminate an additional uncertainty factor introduced in package level.

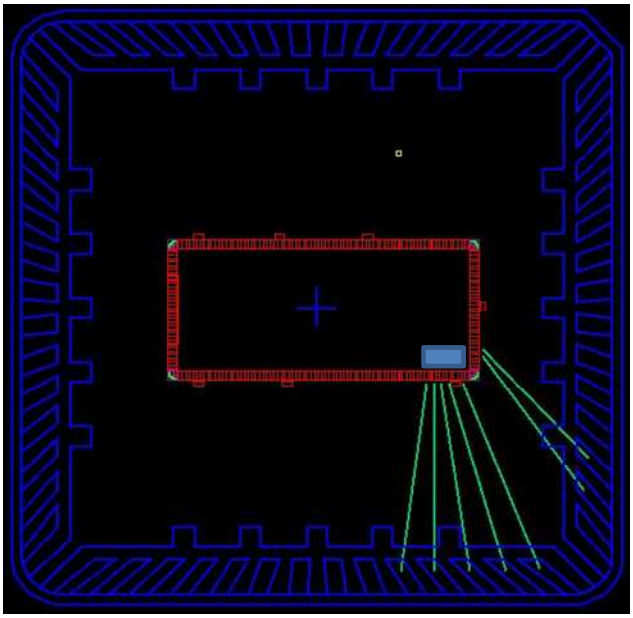

Figure 6: VCO Bondwires

3.2. VCO MEASUREMENT RESULTS

The measurement is performed on an FR-4 test board (Figure 7).

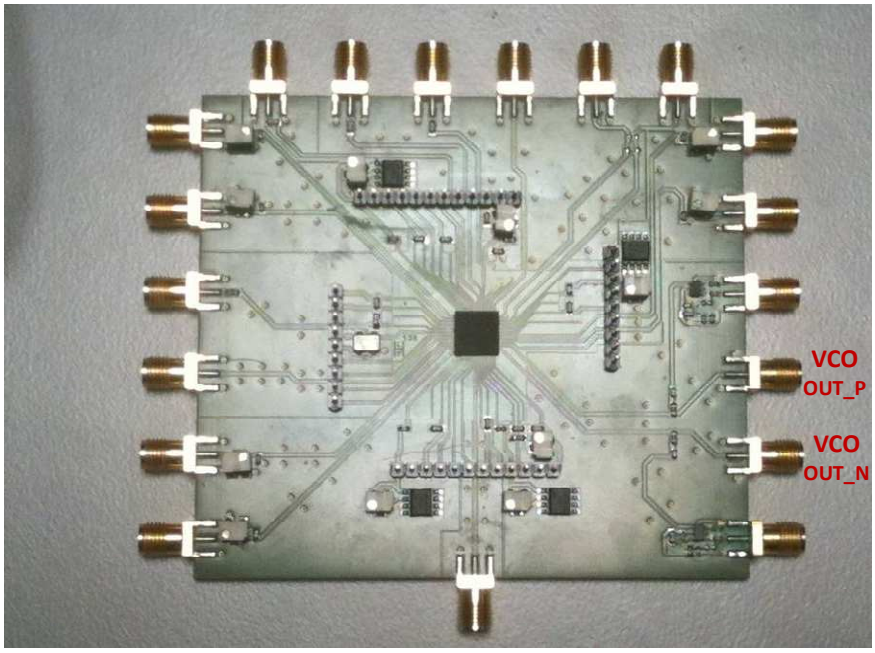

Figure 7: The test board

The table below presents post layout simulation & measurement results of the VCO

Table 1: VCO post layout simulation & measurement results

PARAMETER	SIMULATION RESULTS	MEASUREMENT RESULTS
Power Supply	1.2 V	
Tuning Voltage	0-1.2 V	
Number of Bits	6	
Tuning Range (GHz)	1.36 -1.76	1.34 -1.75
Phase Noise (dBc @1MHz)	-111.9	-112.4
Differential Output Voltage Amplitude (mVpp)	360	350
Power dissipation (mW)	2	2.2
Size	840um x 400um	

Figure 8 shows the signal from the VCO as measured with the oscilloscope. When the negative terminal of the VCO drives the 50Ω of the probe, and the positive terminal is terminated to 50Ω, the output peak-to-peak voltage is 177mV.

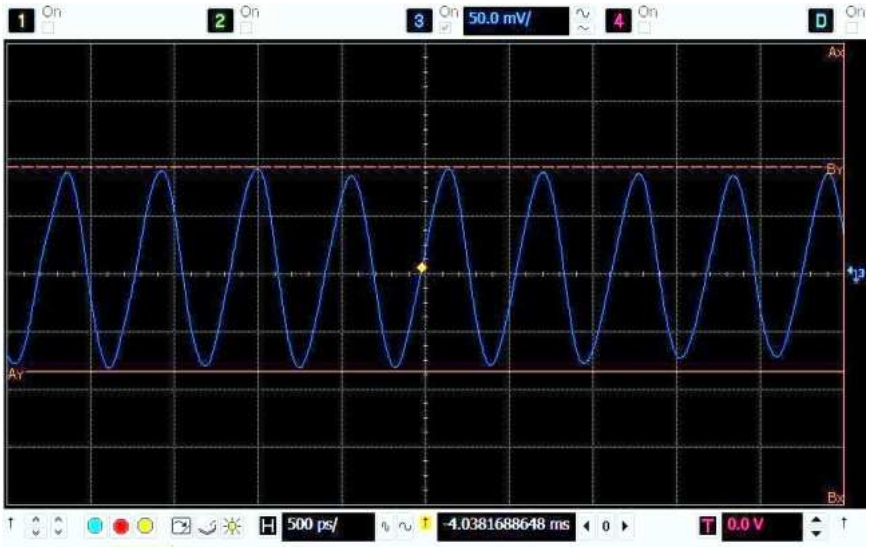

Figure 8: VCO transient signal

The spectrum of the VCO is illustrated in Figure 9, setting the state of the capacitor bank to 0 (All bits 0) and Vtune to 0V.

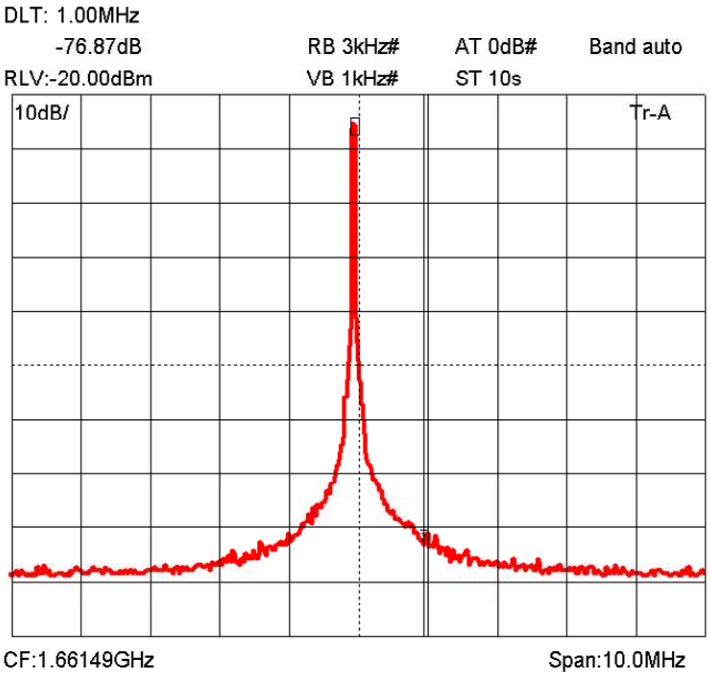

Figure 9: VCO Spectrum

Figure 9 presents simulated and measured results of the VCO tuning range, for various settings of the capacitor bank and the varactor voltage to 1.2V and 0V. Measurement results present a very good correlation to the simulation result, exhibiting a worst case deviation less than 3%.

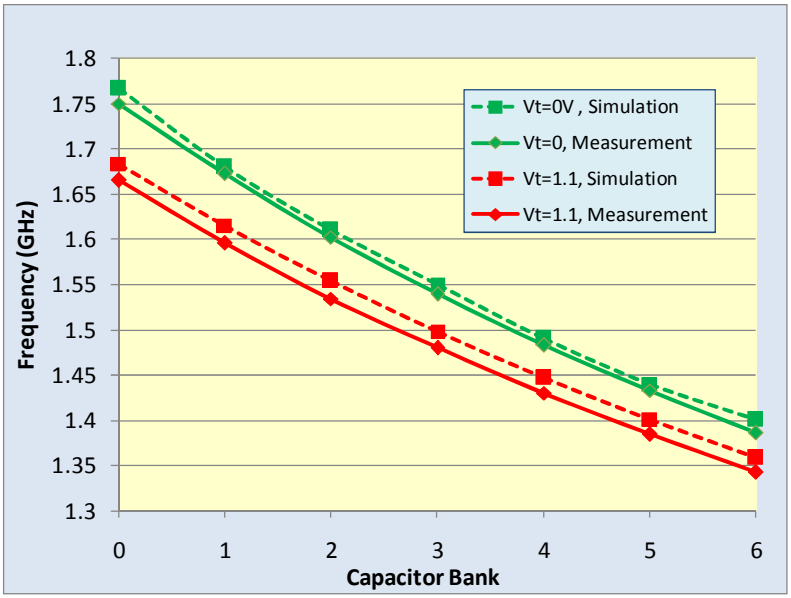

Figure 10: VCO tuning range

The table below presents the phase noise of the VCO.

Table 2: VCO Phase Noise

OFFSET FREQUENCY FROM CARRIER	PHASE NOISE (dBc/Hz)	
	MEASUREMENT RESULTS	SIMULATION RESULTS
100 KHz	-83.2	-83.6
400 KHz	-102.9	-101.1
800 KHz	-108.9	-109.3
1 MHz	-112.4	-111.9

4. CONCLUSIONS

Two EDA toolsets are presented, which introduce an inductance-aware design flow. The fast and accurate prediction of the performance of integrated inductors, RF interconnects lines and bondwires helps minimize the risk of a design failure due to inductive behavior. The flow is seamlessly integrated in a typical RF IC design chain. The modelling methodology is applied to the design of an LC VCO in TSMC 65nm CMOS technology. The accuracy of the presented EDA toolsets is validated through the

agreement between measurement and simulation for the VCO phase noise, tuning range and signal amplitude.

5. REFERENCES

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