Inductor Modeling with Layout-Dependent Effects in 40nm CMOS Process

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***Abstract*— Layout-dependent effects (LDE) as they are encountered in modern semiconductor technology processes are addressed and considered in this work. In particular, their effect on inductor modeling is discussed based on experimental results of devices fabricated and characterized in a 40 nm technology process. The proposed vector based modeling approach is accounting for these effects and its validity is demonstrated by comparison to experimental data. Improved correlation to measured inductor metrics such as inductance L and quality factor Q is demonstrated by considering the layout-dependent effects.**

***Index Terms*— Inductors, nanotechnology, semiconductor device measurement, semiconductor device modeling.**

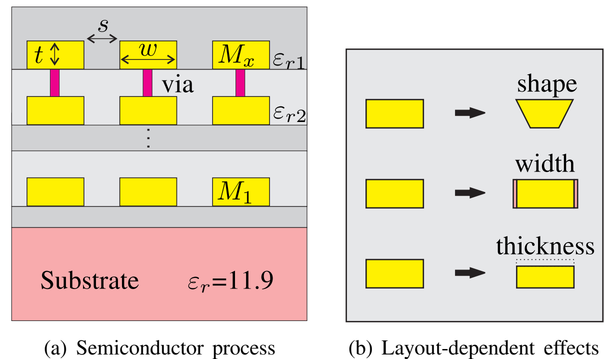
I. Introduction

Device modeling in advanced semiconductor processes, e.g. 65 nm and below, becomes more dependent on the actual device layout itself since metal parameters such as width, spacing, thickness and sheet resistance of the fabricated metal tracks are in relation to the layout density. These pattern related effects may have a significant impact on the fabricated silicon devices such as inductors, capacitors, and interconnects. Semiconductor foundries are addressing these effects by additional technology process characterization work which is provided to their customers in terms of proprietary technology files such as iRCX. Electronic design automation (EDA) tools, whether using electromagnetic solvers or lumped element approaches are expected to deal with such fabrication effects in order to provide accurate and reliable models to IC designers seeking for first pass silicon.

Scope of this work is to present a rapid vector based RLCk extraction methodology which is capable of dealing with layout-dependent effects as they are present in today's semiconductor processes. Inductor design and characterization in a 40 nm process is discussed and comparisons to measurements are shown in order to prove the model validity. Layout-dependent effects as they are typically encountered in a such a technology node are presented and their possible impact on device behavior is discussed. Finally, measurement results of different fabricated inductors are presented and a comparison to modeled data with and without the consideration of layout-dependent effects is performed.

II. Technology Process and Layout-Dependent Effects

Semiconductor processes typically support multiple metal layers with different thickness and conductivity which are separated by several dielectric layers between them. Metal interconnects called vias are ensuring proper electrical contact between consecutive metal layers if needed. A simplified cross section of such a stack-up is depicted in Fig. 1(a). Metal segments on the same layer



(a) Semiconductor process (b) Layout-dependent effects

Fig. 1. Simplified cross section of back-end in semiconductor process and layout-dependent effects (LDE) for metal tracks.

share physical properties such as metal type (copper or aluminum), metal thickness t while they are surrounded by a dielectric material with permittivity ε_r. Metal width w and spacing s are not uniform, since these are layout dependent parameters. As technology nodes are moving into the region of 40 nm and below fabrication effects become more dominant and have to be taken into account. At these technology nodes, metal and process material parameters deviate from their nominal values since they depend on user defined layout parameters. In other words, drawn metal width and spacing as given in the layout will be different from what is going to be fabricated in real silicon. Additionally, even material parameters such as metal thickness t and sheet resistance R_s depend on the surrounding metal density. The layout-dependent effects with the greatest impact on the electrical properties, as shown in Fig. 1(b), are summarized below.

- Top-Bottom Bias: Metal segments have no longer or-

thogonal cross-sections but rather trapezoidal shapes. Top and bottom biasing is applied to capture this effect which has an impact mainly on segment inductance and coupling capacitance to adjacent segments.
- Width Enlargement: Metal width depends on the surrounding metal density and is enlarged according to that. Width enlargement affects all major parameters such as inductance, coupling capacitance and conductor resistance.
- Thickness Ratio: Metal and dielectric thickness depends on layout parameters such as layout density and metal width. Varying thickness is caused by tolerances in the chemical mechanical planarization (CMP) process.
- Resistance: Metal sheet resistance R_s also depends on layout parameters such as metal width and its spacing to adjacent segments. This dependence causes a direct impact on the segment's ohmic losses.

As it is evident by the previous discussion, LDE may have a significant impact on the electrical parameters of the fabricated silicon devices. Ensuring proper modeling for first time right silicon requires thorough technology characterization by the semiconductor foundries. On the other hand, EDA tools assisting IC designers must be able to support such advanced fabrication effects and include them in their modeling algorithms to ensure accurate device model extraction.

III. Vector based RLCk modeling

VeloceRaptor^{TM} (VR) is Helic's core modeling engine and is based on a set of proprietary algorithms. When called up within a layout environment, it scans hierarchically the circuit layout for metal structures, such as integrated spirals, capacitors, and interconnects. A spiral structure or interconnect line is divided into a number of vectors with annotated layer information, referred to as segments.

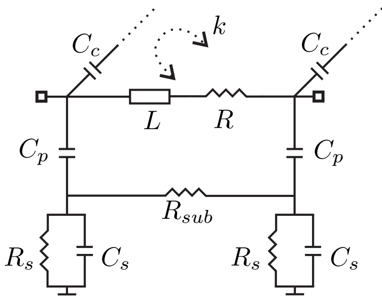


Fig. 2. Equivalent 2-port network for each metal segment of vector based modeling engine.

Each segment is modeled by an equivalent 2-port network [1], as given in Fig. 2, taking into account its self inductance L, ohmic losses R, its parasitic capacitance to the underlying metal layer C_p and the underlying parasitic substrate network formed by R_{sub}, R_s and C_s. Capacitive coupling to adjacent metal segments is ensured by C_c. In particular, mutual inductance among all pairs of segments is modeled with magnetic coupling elements k in the model's netlist and its calculation is based on a vector representation of the currents flowing through segment pairs. To cover conductor skin effect and proximity effects, an adapted network formulation is needed to model the frequency-dependent nature of conductor resistance.

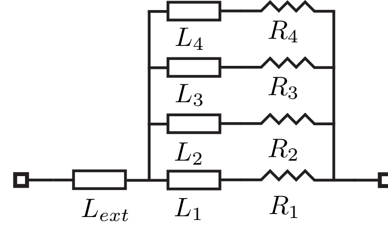


Fig. 3. Ladder network to model conductor skin effect.

The L, R branch of Fig. 2 is therefore substituted by a series L_{ext} and a ladder network of four L_i, R_i elements as given in Fig. 3. To guarantee correctness at DC frequency, R_i values are calculated in such a way so that their parallel combination equals exactly the value of R in the original circuit. This approach allows for modeling of a frequency dependent impedance.

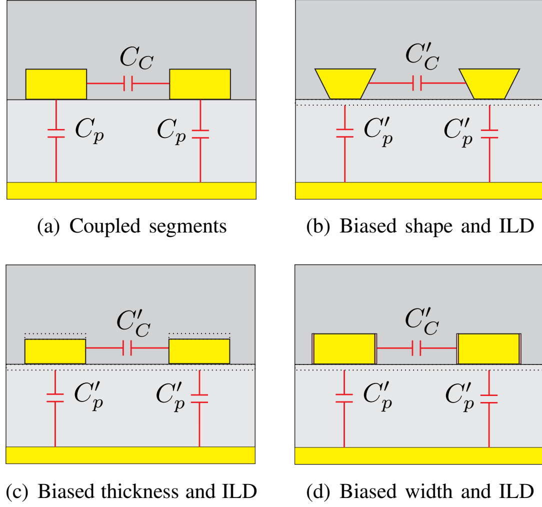
The next step in the modeler's algorithm is the calculation of the mutual inductance values and coupling coefficients k for the whole layout. Only L_{ext} participates in the extraction of mutual inductances to other segments and this self inductance can be described by closed formulas [2]. For two coupled segments with self inductance values of L_a and L_b respectively, a transformer is used in the equivalent circuit model. This transformer is described by its coupling coefficient k, which is determined as

$$k = \frac{M}{\sqrt{L_a \cdot L_b}}, \tag{1}$$

where M is the mutual inductance resulting between both segments [1]. The algorithm calculates an equivalent mutual inductance between every possible pair of segments in the layout. The speed of this modeling technique is attributed to the fact that it is based on closed-form expressions to extract the values of each element in the equivalent model for each segment, as well as for mutual inductances and coupling capacitances. The validity of this modeling approach has been verified by experiment [3] [4].

IV. LDE Impact on Inductor Modeling

As it is evident by the previous discussion, the proposed modeling approach depends on the geometry of the recognized segments within a layout. As a consequence layout-dependent effects as discussed in Section II have a direct impact on the extracted model elements of each

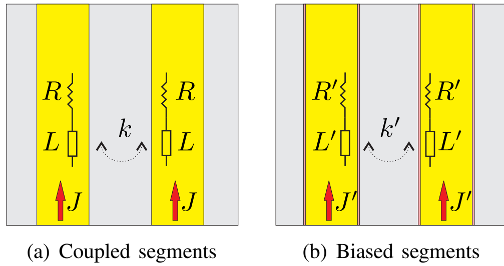


(a) Coupled segments (b) Biased shape and ILD

(c) Biased thickness and ILD (d) Biased width and ILD

Fig. 4. LDE impact on capacitive coupling between adjacent metal segments. Intralayer dielectric (ILD) variation is shown.

segment. In particular, LDE can be investigated in terms of adjacent metal segments as they are encountered in inductors with multiple spiral turns. A cross section of two capacitively coupled segments is shown in Fig. 4(a). Any change in the conductor geometry whether this concerns shape, thickness, or width as seen in Fig. 4(b)-(d) has a direct impact on the amount of capacitive coupling present between conductors since the total electrical charge is altered. In order to retain accurate model extraction the capacitance values in the equivalent networks of the segments have to be adjusted accordingly.



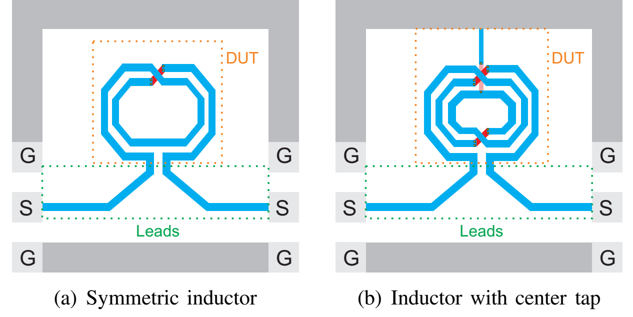
(a) Coupled segments (b) Biased segments

Fig. 5. LDE impact on magnetic coupling and ohmic losses between adjacent metal segments.

LDE have also an impact on the metal's ohmic losses and the amount of magnetic coupling present between adjacent segments as indicated in Fig. 5. Any change on metal geometries has an impact on the conductor's current density J and magnetic flux present between both segments, thus self and mutual inductances expressed by L and k are affected, respectively. Furthermore, the varying sheet resistance which is a function of the layout density has a direct impact on the ohmic losses expressed by R.

V. Inductor Design and Experimental Results

Inductor design for experimental characterization, as shown in Fig. 6, differs significantly from the usual inductor design as used in circuit layouts. The actual device under test (DUT) is extended by interconnect structures also called leads. These metal lines are connecting the DUT terminals with the pads, e.g. in GSG configuration, which are contacted by RF probes during on-wafer measurements.



(a) Symmetric inductor (b) Inductor with center tap

Fig. 6. Example layout of symmetric octagonal inductors fabricated for on-wafer characterization.

Removing the contribution of the leads from the measured data is performed by a mathematical procedure known as de-embedding. Therefore additional characterization structures are needed, e.g. implemented as OPEN and SHORT. The OPEN is formed by the leads which are terminated by open stubs while the SHORT is formed by the leads which are terminated by a transition to the ground plane. Designing well-defined de-embedding structures is essential for accurate device characterization. The mathematical procedure for the OPEN-SHORT de-embedding is a well known method and is described by the following equation

$$Y_{DUT} = \left[[Y_{RAW} - Y_o]^{-1} - [Y_s - Y_o]^{-1} \right]^{-1}, \quad (2)$$

where Y_o and Y_s are the Y-parameter matrices of the measured OPEN and SHORT, respectively.

All measurements shown in this section were taken with an Agilent PNA network analyzer after an LRRM calibration was performed to remove RF probe and cable effects from the measurement setup. The DUTs were fabricated in a 40 nm process with 6 metal layers and one additional AP aluminum layer. As can be seen from the extracted inductor metrics in Figs. 7–9 the impact of the layout-dependent effects results in improved correlation to the measured inductor data. Model deviations Δ are calculated according to $\Delta = abs((Model - Meas)/Meas)$.

Table I summarizes the inductor metrics correlation for the investigated devices. The metrics listed in the comparison table represent the low frequency inductance L_{DC}, the maximum quality factor Q_{max}, and the self

TABLE I

INDUCTOR MODEL TO MEASUREMENT DEVIATIONS IN (%)

Device	w/o LDE					with LDE				
	L_{DC}	$Qmax_{se}$	$Qmax_{diff}$	fsr_{se}	fsr_{diff}	L_{DC}	$Qmax_{se}$	$Qmax_{diff}$	fsr_{se}	fsr_{diff}
W3S2N3	2.5	–	5.0	–	10	2.5	–	0.5	–	10
W4S2N6	3.0	–	2.5	–	3.5	2.5	–	1.0	–	1.5
W5S1N4	2.5	7.0	9.0	2.5	18	1.5	5.5	3.0	2.5	9.0

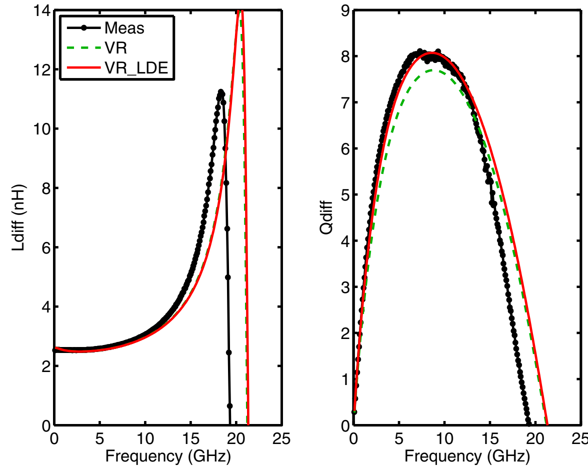


Fig. 7. Measured and simulated metrics for device W3S2N3 with inductor geometry w=3 μm, s=2.5 μm, and turns N=3. Inductor has center tap and only differential excitation $(diff)$ is considered for comparison to measurements.

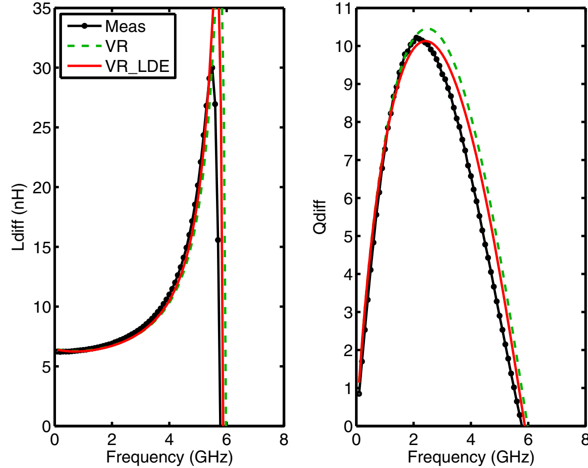


Fig. 8. Measured and simulated metrics for device W4S2N6 with inductor geometry w=4 μm, s=2 μm, and turns N=6. Inductor has center tap and only differential excitation $(diff)$ is considered for comparison to measurements.

resonance frequency f_{SR} of each inductor for single-ended and differential excitation, respectively.

VI. CONCLUSION

A rapid vector based inductor modeling technique is described taking into account layout-dependent effects in a

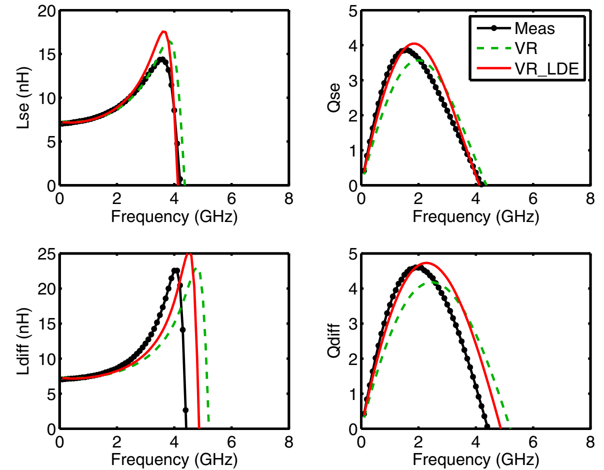


Fig. 9. Measured and simulated single-ended (se) and differential $(diff)$ metrics for device W5S1N4 with inductor geometry w=5 μm, s=1 μm, and turns N=4.

40 nm technology process. LDE may have a significant impact on the fabricated passive silicon devices since drawn metal characteristics such as width and spacing as well as metal properties such as sheet resistance and thickness depend on the actual device layout. Data on fabrication effects, as provided by the semiconductor foundries, have to be taken into account for proper device modeling.

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