RF Passive Device Modeling and Characterization in 65nm CMOS Technology

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Abstract— Rapid passive device modeling is discussed in this work based on test structures fabricated in a 65 nm CMOS process with M1–M9 copper metal layers and one aluminum metal layer AP. Capacitance extraction for overlapping microstrips and shielded microstrip structures is investigated. Individual capacitances are modeled in terms of area and fringe components, either between microstrips or between microstrips and silicon substrate. Good correlation to silicon data is achieved for the fabricated test structures. The validity of the proposed model is also investigated for complex passive devices such as inductors and interdigitated capacitors. Device metrics for both types of passive devices are investigated and compared to measured silicon data. Good agreement is achieved in all cases proving the accuracy of the proposed modeling approach.

Keywords— Semiconductor device modeling, CMOS integrated circuits, inductors, capacitors

I. Introduction

Accurate parasitics extraction and passive device modeling in advanced semiconductor processes is a constantly growing request by integrated circuit (IC) designers, especially in the domain of mixed-signal and RF design. Electronic design automation (EDA) tools are expected to provide accurate and reliable models to IC designers seeking to achieve first pass silicon. Furthermore, rapid extraction and simulation times are crucial parameters for achieving optimum designs and shorter time to market cycles. Specialized RLC parasitic extractors, such as Magma's QuickCap [1] and Synopsys' Raphael [2], use well known electromagnetic theory to extract the parasitics of specific interconnect patterns. Alternatively, planar 2.5D or full wave 3D EM solver solutions based on Finite-Difference (FD), Finite-Elements (FE), and Method of Moments (MoM) [3] are being used for simulation and extraction of device parasitics. Dedicated electromagnetic tools can deliver accurate extraction for different type of interconnection patterns but they usually provide output data which are not directly translated into a SPICE type netlist needed for circuit simulation. Additionally, long extraction times and the limited device types they can handle impose restrictions. Transition from an IC layout environment to an EM solver environment requires significant user interaction. Depending on the device layout and EM solver meshing specifications large simulation times may result. Scope of this work is to present a rapid RLCk extraction methodology [4] which is capable of dealing with generic interconnects as well as any type of passive device supported by today's silicon technologies. Helic's VeloceRaptor modeling engine is seamlessly integrated in the IC design flow [5] and allows for rapid RLCk model extraction for passive devices such as inductors, capacitors, and interconnects. Helic's toolset allows for synthesis and extraction of custom passive devices and interconnects by creating lumped element models which are translated into a SPICE type netlist. In the following sections II-V parasitics extraction for different microstrip configurations is discussed and a comparison to experimental results is presented. In section VI parasitics extraction is discussed for complex passive devices such as spiral inductors and interdigitated capacitors. Each device is examined with corresponding metrics and again experimental data for fabricated devices in the same silicon technology are used as reference for model validation.

II. Semiconductor Process

Semiconductor processes typically support multiple metal layers with different thickness and conductivity which are separated by several dielectric layers between them. Integrated passive devices such as inductors and capacitors can be designed by combining different metal layers. Metal contacts and vias are ensuring proper electrical contact between consecutive metal layers if needed. A simplified cross section of such a CMOS technology stack-up is depicted in Fig. 1.

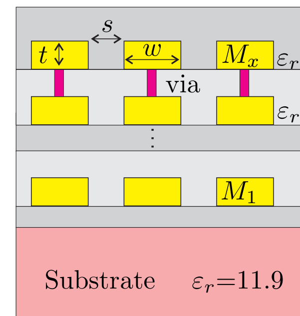


Fig. 1. Simplified cross section of back-end in semiconductor process with multiple metal layers.

Metal lines on the same layer share electrical properties such as sheet resistance R_s (Ω/sq) and metal thickness t while they are surrounded by a dielectric material with permittivity ε_r. Metal width w and spacing s are not uniform, since these are layout dependent parameters. Integrated passive devices such as inductors and capacitors used in integrated circuit designs are fabricated preferably using the upper metals to ensure good electrical performance. Inductors are routed with different shapes on

the thicker top metal layers, e.g. copper layer M9=3.4 μm and aluminum layer AP=1.45 μm, to ensure lower ohmic losses. Capacitors on the other side are implemented either as metal-insulator-metal (MIM) structures or as interdigitated metal-oxide-metal (MOM) structures using several metal layers. As technology nodes have moved into the region of 40 nm and below, fabrication effects become more dominant and have to be taken into account. At these technology nodes, metal and process material parameters, as they are given with their nominal values are not always valid since they depend on user defined layout parameters. The designed metal width and spacing as given in the layout will be different from what is going to be fabricated on silicon. Additionally, even material parameters such as metal thickness t and sheet resistance R_s depend on the surrounding metal density. Passive device modeling with layout-dependent effects is described in [6].

III. Coupled Microstrips

Basic capacitance extraction is considered for parallel metal segments which are treated over a metal plane forming a microstrip like structure, as shown in Fig. 2.

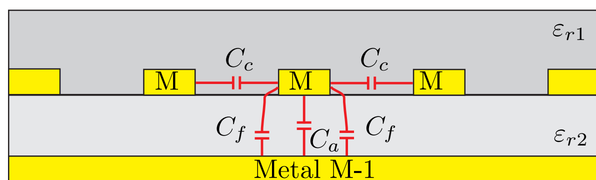


Fig. 2. Cross section of basic conductor pattern for capacitance extraction.

In a more general case this pattern is expanded to multiple layer dielectrics and metals. Capacitive coupling between individual segments is analyzed in partial components as shown in Fig. 2. Area capacitance C_a represents the overlapping part between individual metal tracks and underlying metal planes which form a parallel plate capacitor. The fringe capacitance C_f represents the contribution of the conductor side walls and is added to C_a to form the total overlap capacitance between each conductor and its underlying metal plane. Coupling capacitance C_c between adjacent conductors is computed by taking into account top and bottom plate contribution as well as side wall height. Such basic interconnect capacitances can also be calculated by closed form expressions [7], [8]. The total capacitance for the center victim conductor is expressed by

$$C_{total} = C_a + 2C_f + 2C_c. \tag{1}$$

Analyzing these individual capacitances is performed by a basic coupled microstrip approach as shown in Fig. 3. Capacitances between conductors and between conductor and ground plane are determined by a well known even- and odd-mode analysis. For even-mode excitation, two identical voltage signals are applied between conductors and the common ground plane. The resulting dynamic field lines asymptotically move along the symmetry plane forming what is equivalent to an open circuit (OC) between the two conductors. In such a case the two conductors appear to be isolated from each other and capacitive coupling is present only to the underlying ground plane.

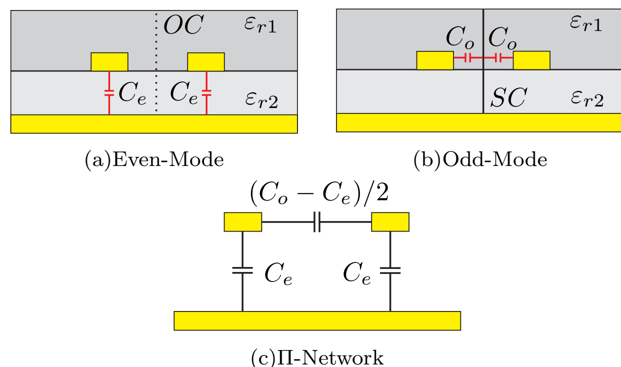


Fig. 3. Even- and odd-mode analysis for coupled microstrip conductors and equivalent Π-network.

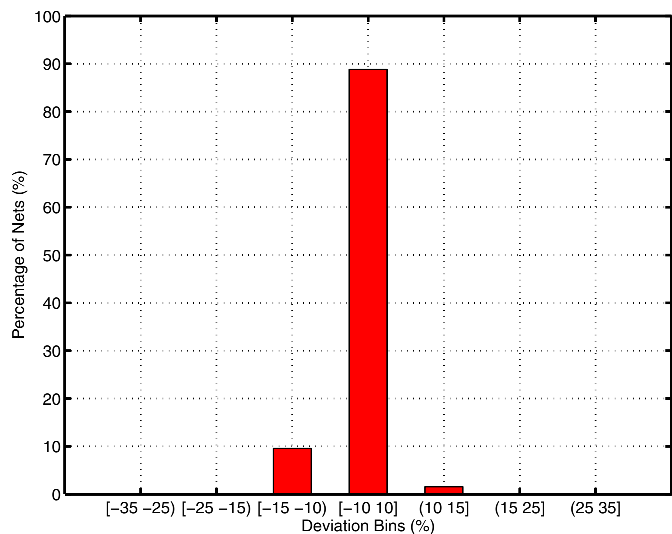


Fig. 4. Deviation of modeled and EM solver based total capacitance C_{total} for a 9-metal 65 nm CMOS process. A total number of 4445 experiments is used for comparison.

The so called even-mode capacitance is stated as C_e including area and fringe components for each conductor and can be calculated as in [9]. For odd-mode analysis two voltage signals of same amplitude and opposite phase are considered between conductors and ground. Dynamic field lines starting from the positively charged conductor will terminate on the surface of the adjacent negatively charged conductor. As a result, the symmetry plane between the two conductors acts as a short circuit (SC) concentrating dynamic field lines between conductors. The resulting capacitive coupling consists of different parts, e.g. bottom and top plane components as well as an area component between the two facing conductor sidewalls. Total odd-mode capacitance is stated in this case as C_o. The equivalent capacitive Π-network in Fig. 3 is formed in terms of self and mutual capacitances as derived from the previous analysis. Using the equivalent network of Fig. 3 following

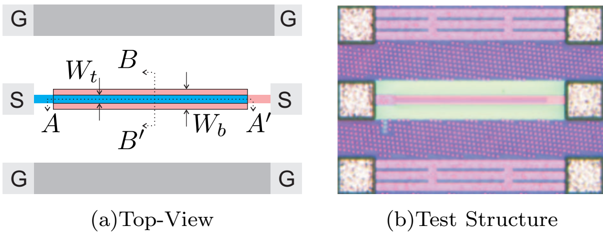
expressions for the individual capacitances are derived [10]

$$C_c = (C_o - C_e)/2 \tag{2}$$
$$C_f = C_e - C_a. \tag{3}$$

This coupled microstrip line approach can be evaluated by comparing the modeled total capacitance C_{total} to the capacitance look-up tables provided for the PDK. Electromagnetic field solvers such as Synopsys' Raphael are typically used for capacitance extraction of such patterns. In Fig. 4 the deviation $\Delta C = [(VeloceRaptor - Raphael)/Raphael]$ of the extracted total capacitance C_{total} for a 65 nm CMOS process is given. The model deviation is displayed in error bins on the x-axis while the corresponding percentage of nets is given in the y-axis. The geometrical parameters for this test pattern vary from width=0.2 μm-12 μm and spacing=0.1 μm-5 μm for all possible layer combinations between M1 and M9. It is seen that for this broad range of geometries most of the test patterns lie within the ±10 % deviation range.

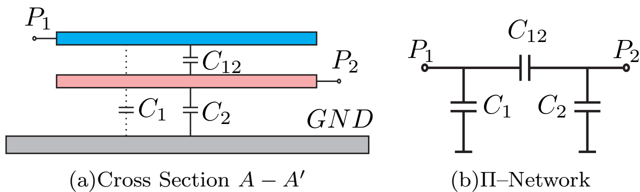
IV. Overlapping Conductors

Capacitance extraction between overlapping microstrips with varying widths is addressed by the experiment in Fig. 5. All test structures are fabricated in a 9-metal 65 nm CMOS process. Top conductor of width W_t on metal layer M9 is connected to port P_1 in GSG configuration with 100 μm pitch distance for on-wafer probing. The bottom conductor of width W_b on metal layer M8 is connected to port P_2, also in GSG configuration. The silicon substrate is forced to ground potential via the GSG box and provides the reference plane for the microstrip conductors under test. In the corresponding cross section of Fig. 6 the capacitance between both conductors C_{12} and the capacitances between conductors and the substrate C_1, C_2 are identified.



(a)Top-View (b)Test Structure

Fig. 5. Schematic representation and fabricated devices for overlapping microstrip structure with varying metal widths for top and bottom conductor.



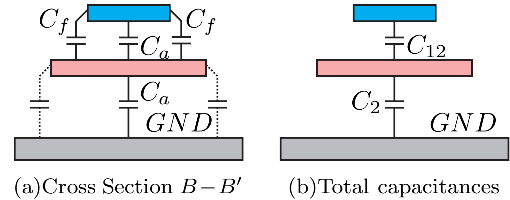
(a)Cross Section $A - A'$ (b)Π–Network

Fig. 6. Cross section of overlapping microstrip structures and associated capacitive Π–network.

Capacitance C_1 from top conductor to substrate is shown with dotted lines since in the fully overlapping case it is masked out by the bottom conductor and can be considered negligible. Since there is no conductive path between ports the equivalent network of this structure is given by a capacitive Π-network as shown in Fig. 6(b). These network elements are readily extracted from measured Y-parameters as given below

$$C_1 = \frac{\Im(Y_{11} + Y_{12})}{2\pi f} \tag{4}$$
$$C_2 = \frac{\Im(Y_{22} + Y_{12})}{2\pi f} \tag{5}$$
$$C_{12} = \frac{\Im(-Y_{21})}{2\pi f}. \tag{6}$$

Looking at the cross section $B - B'$ in Fig. 7 we can identify different capacitance components for area and fringe effects which will help us calculate the total capacitance present between all conductors. Area capacitance C_a is considered to be the plate capacitance formed by the overlap area A of the bottom plate of the top conductor and the top plate of the bottom conductor, which are separated by distance d. Its value can be approximated by the well known parallel plate formula $C_a = \varepsilon_0 \cdot \varepsilon_r \cdot A/d$, where ε_0, ε_r are the dielectric constant of vacuum and the relative dielectric constant of the insulator between both conductors.



(a)Cross Section $B - B'$ (b)Total capacitances

Fig. 7. Cross section of overlapping microstrip structures and associated capacitances.

Fringe capacitance C_f, accounts for conductor side walls, can also be calculated by closed form equations as in [11] and by conformal mapping [12] and is attributed to the closest reference conductor. Awareness of the surrounding conductor pattern is crucial for capacitance extraction since the distribution of electric field lines is a dynamic process. The relative position between conductors and their sizing are used to decide how to distribute the total capacitance present in the network. Corrections are applied to individual capacitance components to avoid double counting, e.g. of fringe capacitance in a multi conductor system. The validity of the proposed modeling approach is proven by comparison to experimental data based on the previously shown test structures. Measurements were taken with an Agilent E8361A vector network analyzer and the on-wafer setup was calibrated with an LRRM routine [13]. OPEN-SHORT de-embedding [14] was performed to remove the GSG pads and leads capacitance for all experiments.

As can be seen in Fig. 8, the proposed model achieves good correlation to measured data for different width ratios

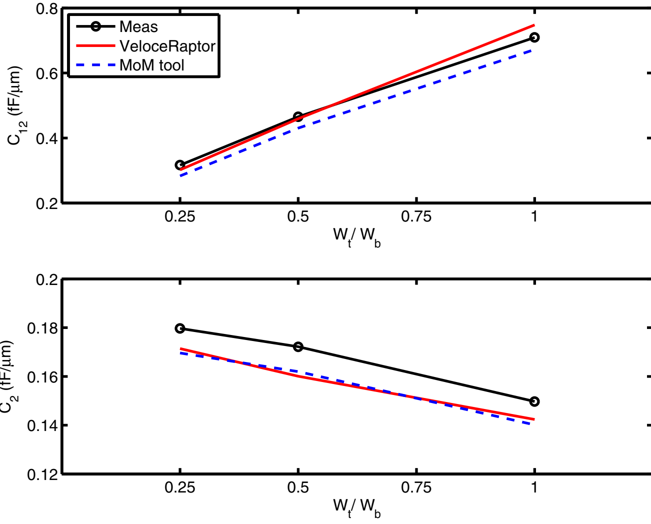
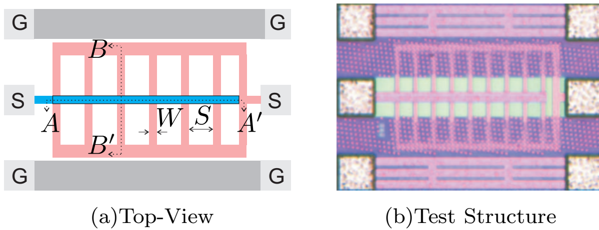


Fig. 8. Experimental results at 300 MHz and model data of VeloceRaptor and third-party MoM tool for per length capacitances of overlapping microstrips. Conductors are on layers M9 and M8 with bottom width W_b=24μm and microstrip line length is L=200μm.

between top and bottom conductor W_t/W_b. As expected, for increasing top width W_t the capacitance between conductors C_{12} is increasing, while capacitance C_2 for bottom conductor is decreasing due to the dominant fringe effect of the closer top conductor.

V. Shielded Conductors

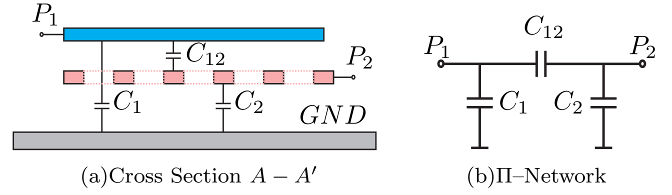
Capacitance extraction for shielded microstrips with varying shield geometries is addressed by the experiment depicted in Fig. 9. Top conductor of width W_t on metal layer M9 is connected to port P_1 in GSG configuration with 100 μm pitch for on-wafer probing. The bottom conductor on metal layer M8 or M1 is forming a shield-like structure, with finger width W and spacing S, connected to port P_2 also in GSG configuration. The silicon substrate is forced to ground potential via the GSG box and provides the reference plane for the microstrip conductors under test.



(a)Top-View (b)Test Structure

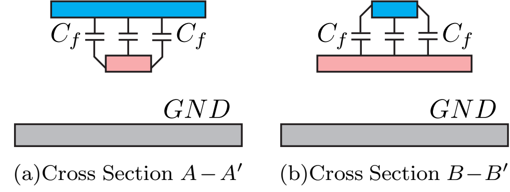
Fig. 9. Schematic representation and fabricated devices for shielded microstrip structures with varying shield geometries.

In the corresponding cross section of Fig. 10, the capacitance between both conductors C_{12} and the capacitances between conductors and the substrate C_1, C_2 are shown. Capacitance C_{12} between top and bottom conductor represents the total capacitance between the two nets, similar to C_2 which represents the total net capacitance between shield structure and substrate.



(a)Cross Section $A-A'$ (b)Π–Network

Fig. 10. Cross section of shielded microstrip structures and associated capacitive Π–network.



(a)Cross Section $A-A'$ (b)Cross Section $B-B'$

Fig. 11. Cross sections for each pair of perpendicular overlapping conductors as encountered in shielded microstrips.

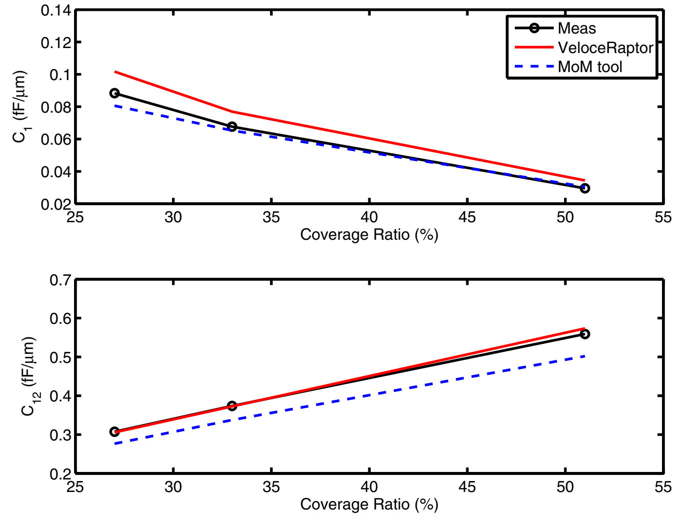


Fig. 12. Experimental results at 300 MHz and model data of VeloceRaptor and third-party MoM tool for per length capacitances of shielded microstrips, finger width is W=6μm on metal M8.

To account properly for the total network capacitances we have to sum up the capacitances resulting from individual overlapping areas of this structure. Area capacitances C_a are calculated as shown before, whereas fringe capacitances C_f for all overlapping segments have to be treated carefully to capture all associated conductor edges as shown in Fig. 11. The combination of both cross sections of Fig. 11 results in proper fringe capacitance calculation for each cross-shaped overlapping conductor pair. Validity of the proposed modeling approach is proven by comparison to experimental data based on the presented test structures. For shielded inductors in CMOS circuit designs, the shield would be forced to ground potential thus C_2 capacitance can be neglected in our test. As shown in Fig. 12 and Fig. 13, the proposed model achieves good correlation to measured silicon data for different coverage ratios, defined as $(N \cdot W)/L$, where N, W, and L are number of shield fingers, finger width and microstrip line length, respectively.

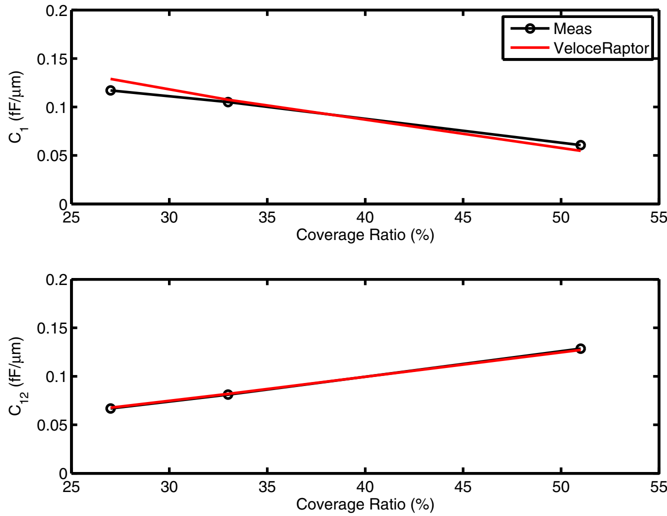
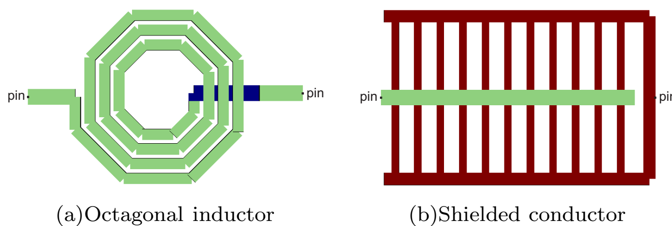


Fig. 13. Experimental results at 300 MHz and model data for per length capacitances of shielded microstrips, finger width is W=6μm on metal M1.

The coverage ratio provides a metric of shielding density and serves as a parameter for describing the electromagnetic effects associated with the shielded microstrip. For increasing shield density the capacitance C_1 between microstrip conductor and substrate fades away while capacitance between microstrip and shield C_{12} is increased. In other words, the shield is capturing the majority of the dynamic field lines as its density increases and after some point makes the substrate invisible to the microstrip line. This electromagnetic effect is used in designs of shielded inductors, where the grounded shield on a lower metal layer is preventing interaction between the inductor and the underlying lossy silicon substrate. The effect of shielding is manifested by an increased inductor quality factor.

VI. RLCk Extraction for Passive Devices

VeloceRaptor is an efficient RLCk modeling engine, with a layout environment interface. It can produce high-frequency SPICE models for almost any metal interconnect or passive device arrangement on silicon. A passive device is divided into a number of vectors with annotated layer information, referred to as segments. Examples of different passive devices and the outputs of the geometry segmentation algorithm are shown in Fig. 14.



(a)Octagonal inductor (b)Shielded conductor

Fig. 14. Output of geometry segmentation algorithm, for different passive devices, as implemented in VeloceRaptor. Individual metal layers and layer transitions are indicated with different colors.

In a layout environment the IC designer selects some

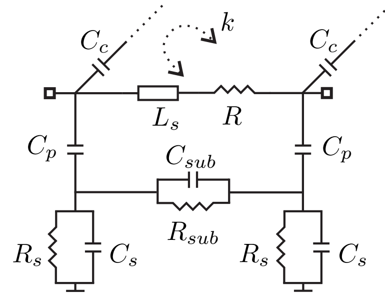


Fig. 15. Equivalent 2-port network for each metal segment of vector based RLCk modeling engine implemented in VeloceRaptor.

terminals on the device or structure to be extracted. The geometry processing starts from the locations of these terminals, also called pins, and proceeds with segmentation of the encountered metal instances. A segment is terminated at each point where a junction, bend, via transition or discontinuity is detected. Each segment is modeled by an equivalent 2-port network, as given in Fig. 15, taking into account its self-inductance L_s and mutual inductance [15] - [17] to other segments through the coupling coefficient k. Broadband ohmic conductor losses which include skin- and proximity effects can be described by an R-L ladder network [18], represented here for simplicity by R. Overlap capacitance to other metal layers is given by C_p and the underlying parasitic substrate network is described by R_{sub}, C_{sub}, R_s and C_s. Capacitive coupling to adjacent metal segments is ensured by C_c. Inductor modeling with equivalent lumped element networks in CMOS technology is described in [19]. Broadband modeling of complex integrated passive devices can be achieved with such lumped element networks [20].

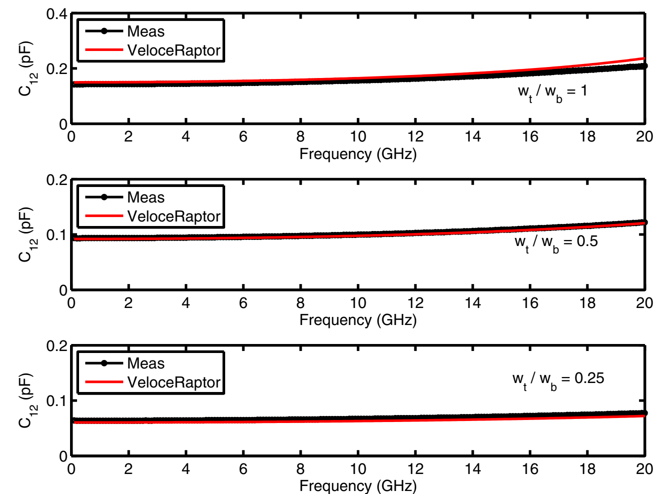


Fig. 16. Experimental results and model data for coupling capacitances of overlapping microstrips (from Fig. 5) on layers M9 and M8. Bottom width is W_b=24μm and microstrip line length is L=200μm.

The previously investigated devices, from Sections IV and V, with overlapping and shielded conductors are now treated with the discussed RLCk modeling approach. The broadband model behavior is obtained by taking into ac-

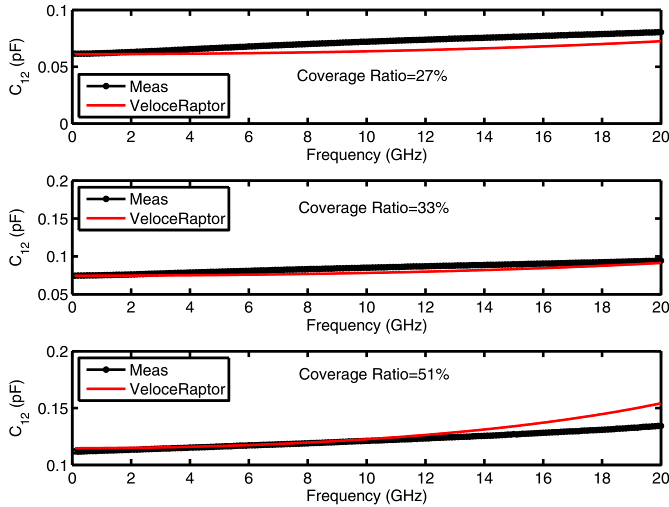


Fig. 17. Experimental results and model data for coupling capacitances of shielded microstrips (from Fig. 9), finger width is W=6μm on metal M8.

count the conductor inductance and the mutual couplings between individual segments. The Y-parameters of the resulting device netlist are calculated and coupling capacitance is extracted over frequency according to (6). Good correlation is achieved for both type of experiments up to 20 GHz, as shown in Fig. 16 and Fig. 17. The previously described capacitance extraction scheme can be also validated on more complex devices such as inductors. Total network capacitance for such a device is the combination of coupling capacitances C_c between conductor segments on the same metal layer and overlap capacitances C_p between the spiral and the silicon substrate. A qualitative metric for estimating the total network capacitance of such a device is the inductor's self resonance frequency (SRF), which is defined as the frequency where the inductance and quality factor become zero. SRF is dominated by combination of the spiral's inductance and its total net capacitance between the spiral and the silicon substrate. Inductors with large outer diameters, multiple turns and wide track widths result in lower self resonance frequency.

TABLE I
INDUCTOR DEVICE PARAMETERS

Device	Type	Width/Spacing	Turns	Stack
1	Octagonal	12 μm / 3 μm	3.5	AP+M9
2	Octagonal	12 μm / 3 μm	3.5	AP+M9+M8

TABLE II
INDUCTOR MODEL TO MEASUREMENTS DEVIATION

Device	Meas. SRF	VeloceRaptor SRF	ΔSRF
1	24.0 GHz	25.8 GHz	7.5 %
2	23.2 GHz	25.3 GHz	9.0 %

The device parameters of the inductors used for this experiment are summarized in Table I. Device metrics of in-

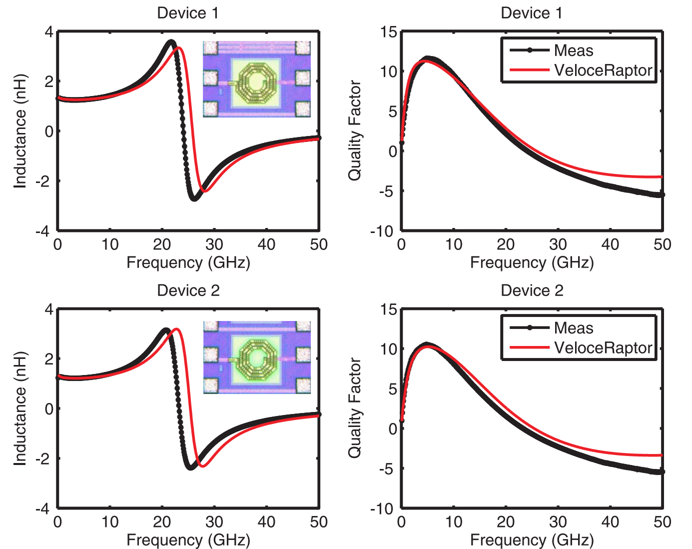


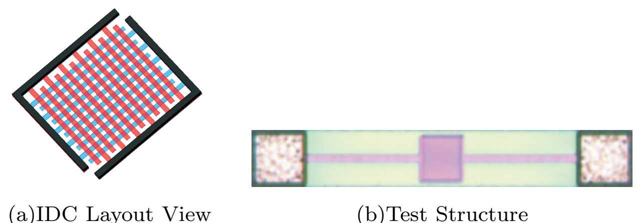
Fig. 18. Experimental results and model data for octagonal inductors fabricated in 65 nm CMOS process.

ductance L and quality factor Q are calculated according to the following set of equations,

$$L = \frac{\Im(1/Y_{11})}{2\pi f} \quad (7)$$

$$Q = \frac{\Im(1/Y_{11})}{\Re(1/Y_{11})} \quad (8)$$

where Y_{11} is the input referred Y-parameter of the 2-port structure. As depicted in Fig. 18 and the values listed in Table II, the proposed model captures well the behavior of the complex inductor devices. Extraction time is another important parameter for each designer since the usual IC design flow requires several optimization cycles in order to fulfill the design goals prior to silicon fabrication. In this context, compact model netlists and fast extraction times are highly desired. The two inductor devices under test are extracted by the VeloceRaptor engine within seconds and described by passive SPICE type netlists of approximately 100 kB allowing for all kinds of frequency and time domain simulations needed in analog and mixed signal designs.



(a)IDC Layout View (b)Test Structure

Fig. 19. Simplified layout view of grid-like interdigitated capacitor and fabricated 6-layers device in 65 nm CMOS process.

Another frequently used passive device is the interdigitated capacitor (IDC). An example of a grid-like IDC which consists of two interdigitated electrode layers having a perpendicular orientation to each other, is given in Fig. 19.

The total device capacitance as determined between the two top metal contacts, shown in black, is a combination of coupling capacitance between electrode fingers on the same metal layer and overlap capacitance between the cross-shaped fingers on different layers. The previously described modeling approach achieves excellent agreement to measured silicon data as shown in Table III. The broadband model performance of the capacitor is compared to measurements in Fig. 20, where scattering parameters are displayed on a Smith chart.

TABLE III
Capacitor Model to measurements deviation

Device	Meas. C	VeloceRaptor C	ΔC
IDC	4.66 pF	4.80 pF	3.0 %

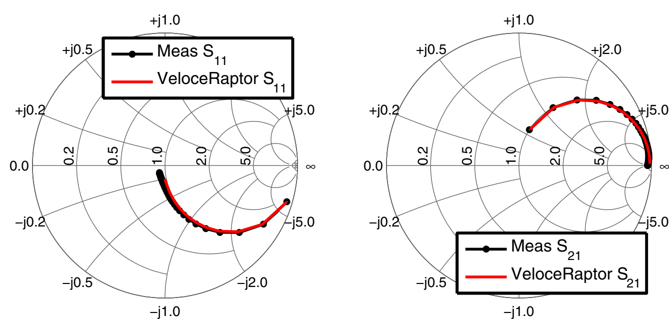


Fig. 20. Experimental results and model data up to 5 GHz for MOM capacitor fabricated in 65 nm CMOS process.

The port-to-port coupling and the reflection at port 1 are described by the S-parameters S_{21} and S_{11}, respectively. Magnitude and phase relations are captured properly by the proposed model.

VII. Conclusion

Passive device characterization and modeling, as needed in a modern CMOS design flow, is addressed in this work. A rapid RLCk extraction engine, VeloceRaptor, is presented and is shown to have adequate accuracy compared to silicon data (from a 65 nm process). A basic interconnect structure is used initially for model validation by comparison to data from an EM solver. Good correlation is achieved for a broad range of geometries and layer combinations. Overlapping and shielded microstrip structures are also investigated in terms of capacitance extraction. Each pair of conductors is analyzed in terms of area and fringe capacitances which are calculated with closed-form expressions. Capacitance calculation is adapted dynamically taking into account the relative positions and orientation of conductor pairs. The proposed modeling approach is initially validated by microstrip test structures which exhibit good correlation to a commercial MoM tool and to measured silicon data. Furthermore, complex passive devices such as inductors and interdigitated capacitors are used to benchmark model accuracy. Modeled and measured device metrics for both inductors and IDC show good correlation and prove the validity of the modeling approach.

Acknowledgment

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