Integrated RF transformer and power combiner design in 150nm CMOS process

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***Abstract*—An integrated passive power combiner is discussed and characterized based on test structure fabricated in a 150 nm LFoundry CMOS process. The power combiner uses differentially driven coupled transformers as a basic building block. We discuss first the constraint driven sythesis of the transformer itself and the device modeling with a rapid RLCk model extractor. Helic's electronic design automation (EDA) tools are used for both, synthesis and extraction of the passive devices. The accuracy of the extracted transformer model is proven by comparison to an EM tool. The fabricated power combiner structure is finally extracted with the same EDA toolset and compared to measured data from on-wafer experiments. Good agreement is achieved in all cases proving the accuracy of the proposed synthesis and extraction methodology for complex RF IC designs.**

I. Introduction

Passive device modeling in advanced semiconductor processes is a constantly growing request by integrated circuit (IC) designers, especially in the domain of mixed-signal and RF design. Electronic design automation (EDA) tools are expected to provide accurate and reliable models to IC designers seeking to achieve first pass silicon. Furthermore, rapid extraction and simulation times are crucial parameters for achieving optimum designs and shorter time to market cycles. Planar 2.5D or full wave 3D EM solver solutions based on Finite-Difference (FD), Finite-Elements (FE), and Method of Moments (MoM) are used for simulation and extraction of passive devices. The electromagnetics behind these methods are well established and yield the needed accuracy, but long extraction times constrain the device type they can handle. Depending on the device layout and EM solver meshing specifications large simulation times may result. Scope of this work is to present a rapid device synthesis and extraction methodology which is capable of dealing with generic interconnects as well as any type of passive device supported by today's silicon technologies. Helic's VeloceRaptor modeling engine is seamlessly integrated in the IC design flow [1] and allows for sythesis of custom devices and rapid RLCk model extraction for passives such as inductors, transformers, and interconnects. Helic's toolset allows for synthesis and extraction of custom passive devices by creating lumped element models which are translated into a SPICE type netlist. In the following sections a design of an integrated passive combiner structure is presented based on coupled transformer devices. The constraint driven transformer design is described in Section II. In Section III a transformer device is used for the extraction of an equivalent passive model with VeloceRaptor. Finally, in Section IV the proposed power combiner topology is discussed and its simulated performance is compared against on-wafer silicon measurements.

II. Constraint Driven Transformer Design

Designing complex passive devices such as integrated transformers in not an easy task even for an experienced IC designer. Numerous and often competing design and optimization parameters have to be considered, such as device size, losses, matching conditions and transformation ratio. Helic's EDA tools allow for a constraint driven transformer design in order to meet the desired design goals across a variety of parameters. Assuming a differentially driven transformer, we begin with the circuit topology shown in Fig. 1.

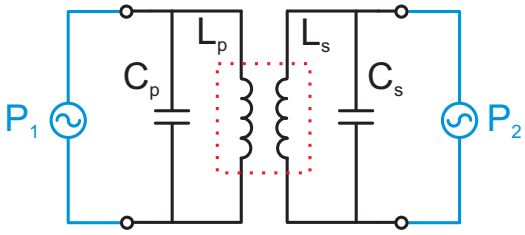


Fig. 1. Circuit topology for constraint driven automated transformer design with Helic's EDA tools.

The primary L_p coil is terminated by the shunt capacitor C_p, while the secondary coil L_s of the transformer structure is terminated by C_s, respectively. These two capacitors are used for achieving optimum impedance matching at the desired center frequency. Let T be a given transformer instance described by a scattering parameter matrix $S(i)$ or Z-parameter matrix $Z(i)$, for a set of M frequencies,

$$S(i) = \begin{bmatrix} S_{11}(i) & S_{12}(i) \\ S_{21}(i) & S_{22}(i) \end{bmatrix}, Z(i) = \begin{bmatrix} Z_{11}(i) & Z_{12}(i) \\ Z_{21}(i) & Z_{22}(i) \end{bmatrix} \quad (1)$$

where i contains all frequencies, $i = (1, \cdots, M)$. Transformer metrics such as primary coil inductance L_p and quality factor Q_p and secondary coil inductance L_s and quality factor Q_s as well as the coupling factor k can be calculated by the following set of equations

$$L_p(i) = \frac{\Im(Z_{11}(i))}{2\pi f}, \quad Q_p(i) = \frac{\Im(Z_{11}(i))}{\Re(Z_{11}(i))} \quad (2)$$

$$L_s(i) = \frac{\Im(Z_{22}(i))}{2\pi f}, \quad Q_s(i) = \frac{\Im(Z_{22}(i))}{\Re(Z_{22}(i))} \quad (3)$$

$$k(i) = \frac{\Im(Z_{21}(i))}{\sqrt{\Im(Z_{11}(i)) \cdot \Im(Z_{22}(i))}}. \quad (4)$$

The shunt capacitors C_p and C_s for loading the primary and secondary inductance, respectively, are used for tuning the

transformer to the desired frequency. Considering the shunt capacitors as a 2-port network allows us to describe them by a scattering matrix $S_c(C,f)$ of the following form

$$S_c(C,f) = \frac{1}{y(C,f)+2} \cdot \begin{bmatrix} -y(C,f) & 2 \\ 2 & -y(C,f) \end{bmatrix}, \quad (5)$$

where $y(C,f) = \jmath 2\pi f C$ is the complex frequency dependent capacitor admittance. The corresponding T-parameter matrix is then given by

$$T_c(C,f) = \frac{1}{2} \cdot \begin{bmatrix} -y(C,f)+2 & -y(C,f) \\ y(C,f) & y(C,f)+2 \end{bmatrix}. \quad (6)$$

The T-parameter matrix of the entire tuned transformer circuit T_{tun}, as shown in Fig. 1, for all frequency points, is then given by cascading the individual T-matrices

$$T_{tun}(C_p, C_s, i) = T_c(C_p, i) \times T(i) \times T_c(C_s, i) \quad (7)$$

and the final S-parameter matrix S_{tun} is obtained by a simple T-to-S matrix transformation

$$S = \begin{bmatrix} T_{12}/T_{22} & (T_{11}T_{22} - T_{12}T_{21})/T_{22} \\ 1/T_{22} & -T_{21}/T_{22} \end{bmatrix}. \quad (8)$$

The IC designer can choose between a variety of design goals such as the the primary and secondary coil inductances and the load impedances at both terminals. Alternatively, optimization goals for the maximum affordable insertion loss and minimum return loss can be entered along with some size constraints and capacitor value constraints. The above set of equations define a constrained optimization problem, which can be solved by algorithms for derivative-free optimization with nonlinear inequality constraints [2]. Such algorithms construct linear approximations to the objective and the constraint functions by interpolating between the vertices of a n-dimensional simplex. In our case, where the variables are the tuning capacitors C_p and C_s, we have n=2. Exiting this optimization routine is achieved as soon as the objective value is minimized and all constraints are non-negative. The basic steps of this optimization routine are summarized below:

Constraint Driven Transformer Optimization Routine

1) Obtain reference S-parameter matrix for 50 Ω loads
2) For each frequency $f(i)$
   - calculate S-parameter matrix of tuned transformer
   - perform arbitrary load conversions on S_c matrix to obtain tuned S-parameter matrix S_{tun}
   - perform bandwidth calculation on S_{tun} to obtain corner frequencies
3) Calculate objective function $S_{tun}(i)$
4) Calculate constraints
   - constraints on insertion- and return-loss, constraints on bandwidth, constraints on tuning capacitors
5) Design goals and constraints true?
   - NO → go back to Step 2) and modify C_p, C_s
   - YES → return transformer geometry and tuning capacitor values (C_p,C_s)

Let's consider a design example of a differentially driven transformer as in Fig. 1, targeted to operate at a frequency f_0=3 GHz, with load and source impedances of 50 Ω, a maximum insertion loss $IL \leq 1$ dB for a 1-dB bandwidth of 50 MHz, and a device area smaller than 400×400 μm^2. The output of the optimizer routine is the layout of the transformer structure itself and the values of the tuning capacitors C_p=0.833 pF and C_s=0.610 pF. Looking only at the resulting transformer topology we can extract the metrics of inductance and quality factor for both the primary and secondary coils of the transformer, according to Eqs. (2),(3), as shown in Fig. 2.

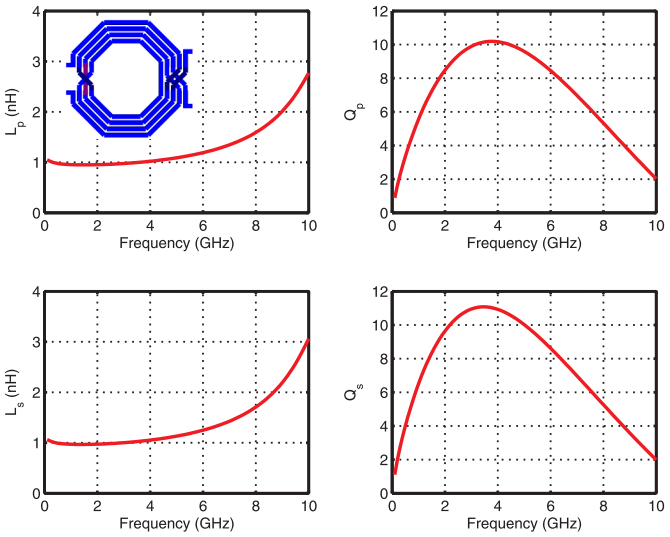


Fig. 2. Simulated inductance and quality factor metrics for primary and secondary coils of synthesized transformer.

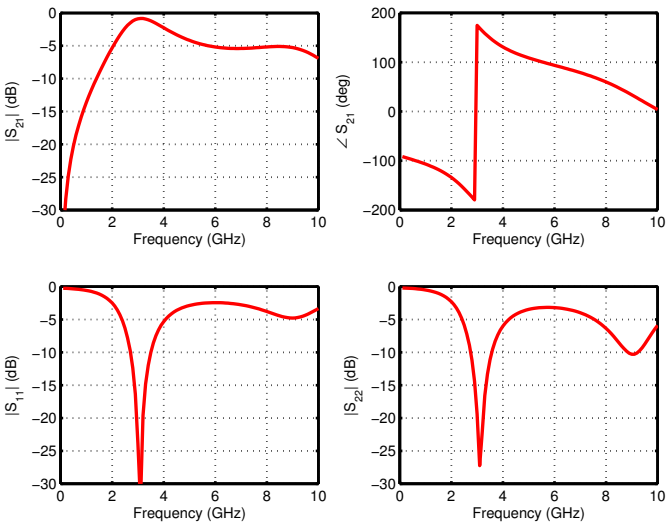


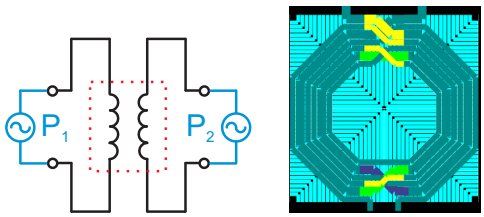
Fig. 3. Simulation results of tuned transformer topology as synthesized by Helic's constraint driven automated design flow.

In order to obtain a transformer that is tuned at the desired operating frequency we have to introduce the capacitors C_p and C_s into our device. Shunting the transformer ports with the capacitors, as shown in Fig. 1, is the final step in the transformer design. The validity of the design flow can be observed by simulating the proposed circuit topology and

looking at the resulting S-parameters, as displayed in Fig. 3. It is readily seen that the transformer device is tuned to operate at the target frequency of 3 GHz, while achieving an insertion loss of less than 1 dB. At the same time the area of the transformer device is within the specified limit. Starting from the design specifications, we have successfully demonstrated the validity of the entire transformer design flow.

III. RLCk Model Extraction

An integrated transformer is a versatile microwave device for designing RF circuits since it can be used for non-galvanic AC signal coupling and impedance transformation. Helic's EDA toolset allows for constraint driven synthesis of several types of transformers. In Fig. 4(a) a differentially driven transformer is shown consisting of a primary coil between port P_1 and a secondary coil between port P_2. The two inductors may be routed in an overlapping pattern at different metal layers or as interleaved spirals at the same layer, as indicated in Fig. 4(b).



(a) Transformer (b) Device layout

Fig. 4. a) Schematic of a transformer consisting of two differentially driven inductors and b) layout of an interleaved shielded transformer device.

In both cases, the electromagnetic coupling between the spirals results in the desired power transfer. The turn ratio between the two spirals also determines the potential and impedance transformation.

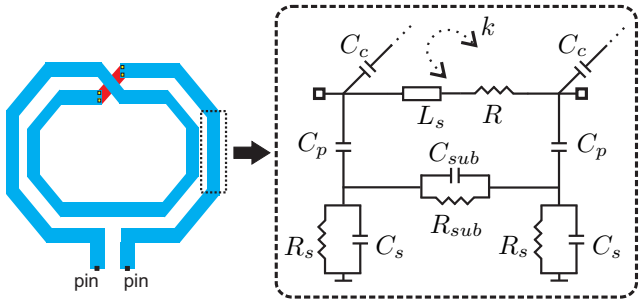


Fig. 5. Equivalent 2-port network for each metal segment of vector based RLCk modeling engine implemented in VeloceRaptor.

All Helic tools are based on VeloceRaptor an efficient RLCk modeling engine, which produces high-frequency SPICE models for almost any metal interconnect or passive device arrangement on silicon. The IC designer selects some terminals on the device or structure to be extracted. The geometry processing starts from the locations of these terminals, also called pins, and proceeds with segmentation of the encountered metal instances. A segment is terminated at each point where a junction, bend, via transition or discontinuity is detected. Each segment is modeled by an equivalent 2-port network [3], as given in Fig. 5, taking into account its self-inductance L_s and mutual inductance to other segments through the coupling coefficient k [4], [5]. Broadband ohmic conductor losses which include skin- and proximity effects can be described by an R-L ladder network [6], represented here for simplicity by R. Overlap capacitance to other metal layers is given by C_p and the underlying parasitic substrate network is described by R_{sub}, C_{sub}, R_s and C_s. Capacitive coupling to adjacent metal segments is ensured by C_c. Passive device modeling with equivalent lumped element networks in CMOS technology is described in [7] – [9]. Broadband model correlation with such networks has been reported in [10]. The validity of the proposed modeling approach is proven by using the designed transformer device as a test structure. Our device model is compared to the extracted model from a commercially available EM simulator. Using differential excitation at the transformer terminals results in the simulated scattering parameters given in Fig. 6. As can be seen, the correlation of the two models is very good while the extraction time for the VeloceRaptor/X model is outperforming the EM tool by orders of magnitude.

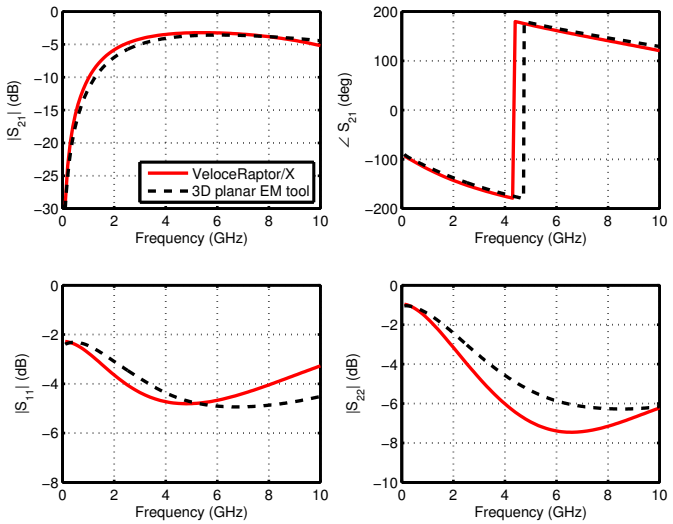
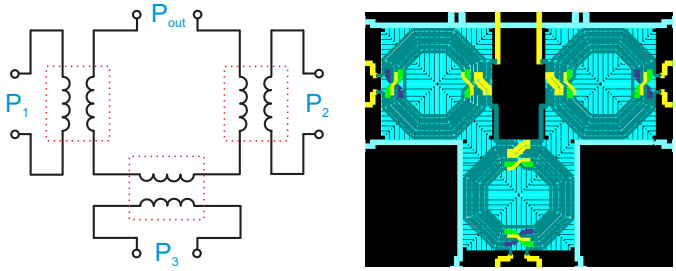


Fig. 6. Comparison of simulated S-parameters between models generated with VeloceRaptor/X and a third-party EM tool.

IV. Passive Combiner and Experimental Results

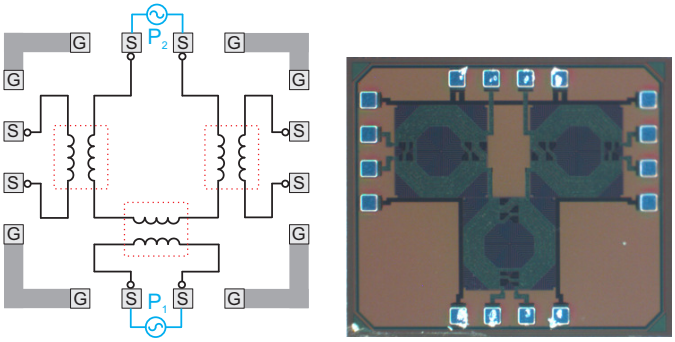
The proposed power combiner consists of three coupled transformers with their primary spirals acting as input ports $P_1 - P_3$ and their secondary spirals forming a ring structure combining the induced power from all input ports, at the output port P_{out}. A schematic representation of this combiner topology is given in Fig. 7. For the on-wafer silicon experiments GSSG pads are used at all combiner terminals as shown in Fig. 8. The measurements setup was calibrated by an SOLT routine [11] and a 4-port network analyzer.

A comparison of measured and simulated S-parameters is given in Fig. 9. The overall bandpass performance of the power combiner structure is captured well and some minor discrepancies in the resonance behavior are most likely due to the missing de-embedding structures on the chip. The contact resistance at the probe to pads interface and the capacitive coupling between probe tips and pads can not be removed due to missing de-embedding structures. Nevertheless, amplitude



(a) Combiner schematic (b) Combiner layout

Fig. 7. Schematic representation of proposed power combiner and layout of test structure.



(a) Measurement setup (b) Silicon die

Fig. 8. Setup for silicon experiments of test structure fabricated in 150 nm CMOS.

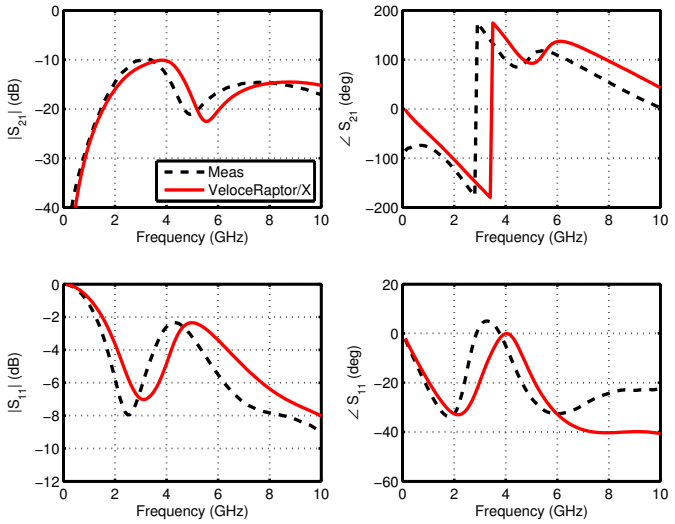


Fig. 9. Measured silicon data and simulated performance of passive combiner model extracted with VeloceRaptor.

and phase relations of the transmitted and reflected signals are modeled properly. The entire test structure including the GSSS pads and ground terminals have been included in the extracted model. The resulting SPICE RLCk netlist consits of approximately, 7.5k resistors, 11k capacitors, 3.8k inductors and 185k mutual inductors. Extraction time for this complex device is approximately 10 s on a PC with a 6-core CPU.

V. Conclusion

An integrated passive power combiner device is designed and characterized in this work based on a 150 nm CMOS process. The core building block of the proposed RF power combiner is a differentially driven transformer. A constraint driven transformer design approach is presented in this work based on the implementation of Helic's EDA tools. The passive devices are then modeled by the VeloceRaptor RLCk modeling engine. Rapid constraint driven device synthesis and model extraction is successfully demonstrated. Good correlation is achieved for the transformer device when compared to simulation results from an electromagnetic solver. Finally, the designed transformer device is used to build a power combiner consisting of three coupled transformers. The entire combiner structure is then extracted with the VeloceRaptor/X tool and compared against on-wafer measurements. The accuracy of the proposed design and modeling methodology is proven by the correlation to measured on-wafer silicon data.

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