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Wide-band substrate crosstalk sensor for wireless SoC applications

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ABSTRACT

A CMOS 65 nm substrate crosstalk noise sensor with exceptional performance characteristics was implemented and used in sensing substrate crosstalk noise signals in a wireless communications System on Chip. The sensor is integrated and fabricated onto the same die with a pin grid array packaged ZigBee Transceiver. It provides gain of 6.5 dB in an operating bandwidth from 1 MHz to 4.5 GHz. The −1 dB gain compression point is measured for input signal amplitude of 124 mV. Its unique substrate noise sensing capacity is demonstrated using silicon measurements in an advanced wireless communication System on Chip, implemented in a CMOS process commercially available by TSMC, where a programmable CMOS control logic of 120 kGate acts as the substrate noise transmitter. The full analysis and its standalone performance are also supported with both silicon measurements and advanced radio frequency simulations results, including all RLCk parasitics from the silicon level till the package, the printed circuit board and the full measurement setup. The trends ruling the substrate crosstalk phenomenon in terms of the noise aggressor distance and the switching activity level are confirmed.

1. Introduction

Mixed-signal SoCs (System on Chip) with both analog/RF and digital blocks implemented onto the same die are increasingly developed in many applications and especially in wireless communications and wireless sensor node interfaces. However, integrating these blocks onto the same silicon causes important performance degradation especially in applications requiring fast digital circuits and high performance analog/RF blocks. Fast switching in digital blocks generates noise which is propagated through the common substrate to the analog/RF circuits (demonstrated in Fig. 1). Coupling occurs between a noise transmitter, which is usually a fast switching digital block or blocks, and a noise receiver, which in most cases, is a quite sensitive analog or RF block and takes place due to the capacitive/resistive nature of the substrate and the devices interface (Fig. 1).

The respective substrate crosstalk noise impact is both linear and nonlinear. Signals from the digital blocks are added to the analog signals and are also introduced through mixing to the desired carrier signals spectrum, therefore imposing detrimental effects on the performance of mixed-signal circuits. The described substrate crosstalk induced performance degradation is introduced in systems where digital blocks are integrated in close proximity to sensitive analog and radio frequency (RF) circuits. Therefore, simulating and identifying the critical substrate crosstalk paths can lead to solutions for reducing/optimizing it and improving mixed-signal circuit's performance.

On the application side, currently the general trend of CMOS technology shrink in technology nodes below 28 nm, the extremely dense integration to minimize the product area/cost and the new design concept making analog/RF functions using digital architectures, renders substrate crosstalk as the most crucial problem, especially in the case of technology multi-sourcing. This becomes even more severe in System on Chip (SoC) level, due to complete radio spectrum usage from 3 kHz to 30 GHz and the wireless applications specifications with signal/power below background noise. Things will become even tighter as SOCs move to millimeter wave IC design and from the 4G/LTE (long term evolution) mobile communication to the 5G mobile communication design era.

Several methodologies and modeling approaches [1–12] to simulate substrate crosstalk have been proposed, but currently none is thoroughly validated or adequate enough to address this phenomenon in its right extend due to signal measurement difficulties. Recent analyses and methodologies [13–17], simulate substrate crosstalk both in terms of accuracy and physical phenomenon behavioral trends. On the electronic design automation (EDA) industry status and the respective software tools capabilities, only

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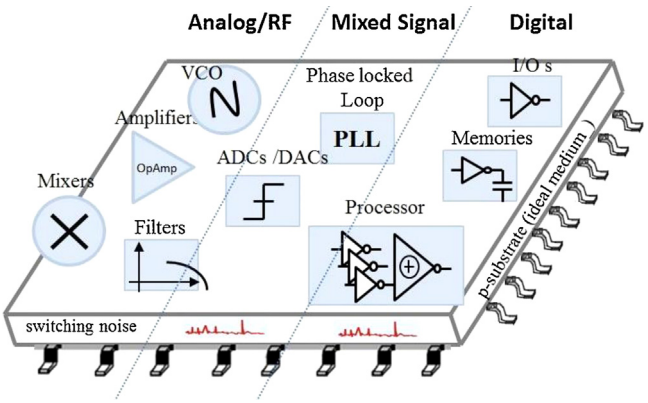

Fig. 1. Representation of a full SoC substrate crosstalk with the related analog, RF and digital and mixed signal blocks integrated onto a common silicon substrate.

two solutions are commercially available [17,18], but both with questionable accuracy. While the need of a substrate coupling aware design flow or a related EDA tool are of extreme importance, an even more challenging and crucial task is to be able to validate if the proposed substrate crosstalk noise simulation methodologies and flows are accurate, correlating simulations with direct measured substrate noise signals and able to identify critical substrate coupling paths. The measurement of substrate and power supply noise enables the monitoring and the analysis of digital switching noise propagation. It is greatly important for understanding substrate crosstalk in several processes, for validating the accuracy of respective EDA tools and simulation techniques and for identifying critical coupling paths across the chip and analyzing the efficiency of various noise suppression methodologies.

In terms of substrate noise sensing, several requirements impose the definition of such a design both in schematic (architecture) and mask design level (layout), as an extremely challenging task. In particular, the sensor should not affect the noise propagation or inject additional noise. The operational bandwidth should be high enough, until 4–5 GHz, so as to capture the high frequency components and low enough to measure the low frequency components. In addition, the sensor should occupy as low active chip area as possible as to enable probing in multiple locations onto the chip. Finally it should be able to multiplex the signals from multiple sensors (since the noise sensing is commonly done in various locations across the chip) in order to reduce the number of the required pins.

Several substrate noise sensing techniques were presented so far in Refs. [18–27]. A simple measurement technique, involved the use of a voltage threshold modulation of a single MOSFET [18,19]. In this technique the substrate noise sensor consists of a single NMOS transistor that senses the substrate noise through the body effect and capacitive coupling to its gate, drain, and source nodes. The specific method is an indirect measurement technique since it is not the substrate noise that is measured but the influence of the substrate voltage on the MOS current. In addition it is extremely limited in terms of the related bandwidth, since bulk driven MOSFET operation can sense signals that have a frequency lower of a few MHz. Nagata et al. [20,21] used voltage comparators as substrate crosstalk noise sensors. A differential latch comparator was used for the substrate noise detector circuits because a high temporal resolution can be expected due to the large gain in positive feedback. An unavoidable drawback of the specific topology is the limitation of probe points mainly due to the large size of these detectors. In addition, this is also an indirect measurement technique since it detects the influence of the substrate voltage on a comparator state. Again, this methodology offers limited bandwidth to some hundreds of MHz, making it unsuitable for wireless communications crosstalk sensing. A more practical topology was also proposed by Nagata et al. [12,22,23]. This topology consists of a source follower (SF) that senses noise voltage and a transistor's transconductance (Gm) that converts the SF's output voltage to current signal. Because of the small device count in this simple front-end structure, it is comparable to a standard flip–flop cell. While this technique enables direct power supply/ground noise to be probed at sufficient points within a digital circuit for mapping noise distributions, again it is limited by a related low operation bandwidth that cannot reach the GHz region and is not suitable for wireless communications SoCs. van Heijningen et al. [24] implemented direct substrate noise measurement circuitries with differential amplifiers to probe substrate and power supply noise with reference to an arbitrary voltage. However the obtained operation bandwidth was in the range of half a GHz. Two extra topologies were also proposed [25,26] based on digital operations, but both were indirect techniques and bandwidth was limited for wireless communications crosstalk paths identification.

The main challenge in wireless SoCs, in terms of substrate noise sensing, is the really broadband gain behavior needed in order to amplify the sensed substrate signals, and capture all the intermodulation's products in the wireless communication GHz region of interest. In addition, the direct substrate noise sensing feature is also required so as to identify sensitive coupling paths. In this paper, a novel design approach of a broadband noise sensor architecture is implemented in a 65 nm CMOS process. A direct and broadband real time sensing topology is provided and its operation is confirmed with silicon measurements on a CMOS 65 nm wireless communication pin-grid array (PGA) SoC, capturing substrate noise injected from a 120 k Gate programmable input–output (IO) and core digital logic, in a frequency range from few MHz to 4.5 GHz. In addition all the essential design specifications are also covered such as the multiplexing capability and the active occupied area.

2. Substrate crosstalk noise sensor

The noise sensor implemented in a 65 nm LP CMOS process by TSMC, is provided in Fig. 2. It is a differential amplifier, with 1.2 V RF transistors M1 and M2 for the differential pair, and with one input connected to a dedicated ground and the other connected onto the substrate so as to implement common mode rejection. The main objectives of the design are a broad band-pass bandwidth response from few MHz over 4 GHz, a satisfactory gain performance and the ability to deliver output single ended signal to the 50Ω load of a spectrum analyzer.

The differential pair M1, M2 is biased through the resistor dividers into the subthreshold region. The DC drain current for an n-channel MOSFET in the subthreshold region is given by Tsividis [27],

$$I_D = \frac{W}{L} I_0 e^{\frac{V_{GS}-V_{th}}{mV_T}\left(1-e^{-\frac{V_{DS}}{V_T}}\right)} = \frac{W}{L} I_0 \times e^{\frac{V_{GS}-V_{th}}{mV_T}} \quad (1)$$

where W/L is the aspect ratio of the transistor, V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltages, respectively, V_{th} is the transistor threshold voltage, and $V_T = k_B T/q$ is the thermal voltage (k_B is the Boltzmann constant, T the absolute temperature, and q the elementary charge). The subthreshold slope parameter m is a technology-dependent constant, usually with a value of $1 < m < 2$, and I_0 is process parameter that also depends on temperature.

The respective transconductance and the drain–source resistance are given below,

$$g_m = \frac{\theta I_D}{\theta v_{GS}} = \frac{I_D}{mV_T} \quad (2)$$

$$r_D = \left[\frac{\theta I_D}{\theta v_{GS}}\right]^{-1} = \frac{mV_T}{\lambda_D I_D} \quad (3)$$

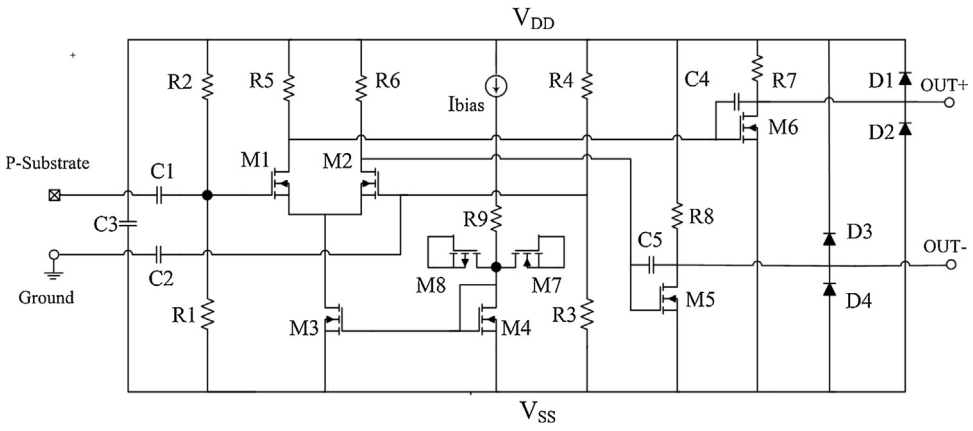

Fig. 2. Substrate noise sensor schematic.

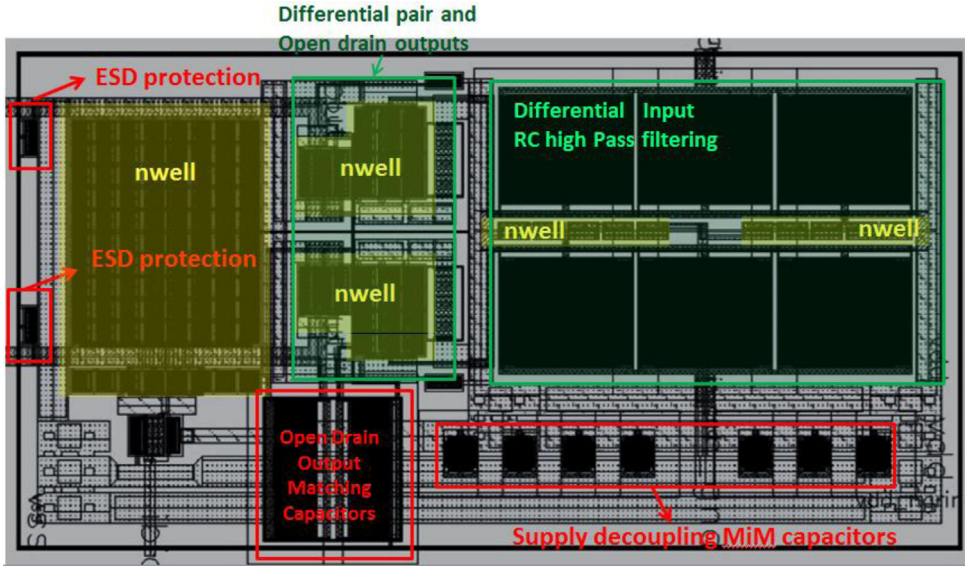

Fig. 3. CMOS 65 nm noise sensor physical design.

where λ_D is the DIBL effect coefficient. The DC gain provided from the differential gain of the proposed topology is provided below,

$$A_{VDC} = \frac{g_{m2}}{\left(\frac{1}{R6}\right) + g_{ds2}} \tag{4}$$

The amplified (by the differential pair stage) substrate and the quite ground reference signals are driven to M5 and M6. These output stages are open drain topologies and were designed with thick gate 2.5 V devices, in order to achieve the 50 Ω driving capability by lowering the output impedance and providing the necessary current to drive the 50 Ω instrument port. R7 and R8 act as pull up resistors for the open drain outputs. The respective gain of these stages cannot exceed 0 dB.

The back end of line metal capacitors C1 and C2 together with the resistor dividers R1, R2 and R3, R4 form high pass filters for the differential input. This high pass CR filter defines the lower cut off frequency of the band pass behavior. The resistance dividers also define the DC operating point of the differential pair. Resistors R5, R6 act as loads. Low value capacitors C4, C5 are used to match the outputs OUT+ and OUT− through the inductances of the SoC PGA package bond wires and M7, M8 and R6 form an ESD protection for the input bias current and D1, D2 and D3, D4 for the differential RF output signals. C3 Metal–insulator–Metal (MiM) decoupling capacitance is placed between the supply power routing rails for supply ripple minimization. A bias current of 750 μA and power supplies of V_{DD} = 1.2 V and V_{SS} = 0 V were used. A respective current mirror topology comprised by M3 and M4 provides the bias current for the differential pair.

In relation to the mask design, the noise sensor layout was fully symmetrical and special attention was given in isolating sensitive devices using biased guard rings. The differential pair and the RC high pass filtering silicon implementation are highlighted in Fig. 3. The differential pair and the output stages had a fully symmetrical layout. All the RF MOSFETs were isolated using inversely biased deep n-well and respective guard rings. All the resistances were designed with separate guard rings. The full sensor footprint lies onto reversely biased deep n-wells (dnw) also highlighted in Fig. 3 and has an active area of 332 μm × 224 μm. Special ESD (electrostatic discharge) protections were designed, using RF devices biased in diode modes. Supply decoupling was implemented using MiM capacitors for active area minimization. The respective layout is given in Fig. 3.

Special attention was paid to each signal and each pin in relation to the isolation of the sensor. The device types that were used and the respective bias settings are provided in Table 1.

Regarding the measurement setup, an off-chip *5320B* broadband transformer (balun), commercially available by Picosecond, was used (and simulated using an s-parameter model provided by the

Table 1
Noise sensor bias settings, pins and devices types.

PIN list		Description
V_{DD}	Positive power supply 1.2 V	"Clean" VDD—no connection to nwell
V_{SS}	Negative power supply 0 V	"Clean" VSS—all the NMOS devices into deep n-wells—each pwell biased to its source DC level (no body effect and no connection to substrate)
vdd_gr	Positive bias of 1.2 V for the deep n-well (DNW) ring surrounding the topology	Separate deep nwell noise isolating ring biasing routed separately to a 1.2 V (no visibility on the s hematic)
Ibias	External current source	DC biasing current 0.75 mA
Ground	Quite ground reference	Separate ground pin available
p-Substrate	Substrate sensing input signal	Substrate noise RF signal captured using a substrate tap
OUT+/−	Positive and negative voltage outputs	Two outputs are delivered through an external balun to the 50Ω load of a spectrum analyzer
Device type list		**Description**
MOSFET	1.2 V NMOS RF/M1–M4, M7–M8	Used in the dif. Pair/nwell ring availability —biased to V_{DD} for pn junction inverse biasing and isolation from substrate
	2.5 V IO NMOS RF/M5–M6	IO 2.5 V std RF NMOS in Deep n-well (DNW) are used at the open drain output stage for electro-migration (EM) reasons
Resistors	RF p^+ polysilicon resistors without silicide/R1–R4	P^+ Poly resistors in n-well without silicide are used for low noise performance/substrate noise coupling minimization
	RF p^+ polysilicon resistors/R5–R8	P^+ Poly resistor in n-well with silicide—high current density capability
Capacitors	RF Mim–capacitor/C3	Placed onto the parallel V_{DD} and V_{SS} routings for area minimization and decoupling
	Metal back end of line (BEOL) capacitors/C1–C2, C4–C5	M2–M5 metal caps for high capacitance density

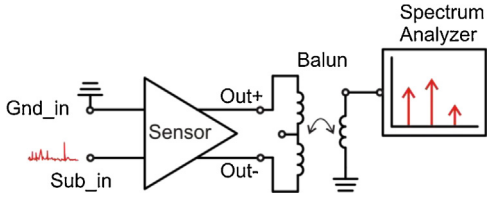

Fig. 4. Measurement setup using a specialized balun and a spectrum analyzer.

supplier) for differential to single ended conversion and in order to drive the sensed signal onto the 50Ω load of the spectrum analyzer. Fig. 4, depicts the measurement setup.

On chip routing parasitics, PGA package and PCB board parasitics were extracted and simulated all in *RLCk* mode using *VeloceRaptor Electromagnetic* (*EM*) modeling engine [28] in order to capture all the performance high frequency effects and ensure silicon functionality. This way complex electromagnetic effects such as self and mutual inductances, frequency-dependent resistance and capacitive couplings were captured.

The noise sensor was designed and simulated using the Cadence suite and the Virtuoso analog/RF custom design flow. The Spectre RF and the high performance APS simulator, also commercially available by Cadence, were used for extracting post-layout simulation results (in nominal conditions and in 25 °C temperature). The related process design kit MOSFET compact model used was BSIM4V4.5. All devices had special RF sub-circuits (RF models) available for running accurate high frequency simulations. The gain versus bandwidth including full RLCk parasitic extraction [28], and adding into the simulation test bench the bond wire package and the PCB board RLCk parasitics model (netlist), is provided in Fig. 5. The substrate crosstalk sensor simulated gain is of a 6.6 dB in an operation band pass bandwidth from 1 MHz to 4.6 GHz.

The respective, through s-parameter simulation, stability factor Kf plot is provided in Fig. 6, depicting that the circuit is unconditionally stable, since the Kf value is above 1 for the whole range of the operating bandwidth.

3. Noise transmitter architecture

The digital noise transmitter (NT) circuit consists of 768 Loop Shift Registers (LSRs) arranged in 32 rows by 24 columns that are controlled and operate through a serial peripheral interface (SPI) bus [29]. A digital circuit with high and externally adjustable switching activity was required. The LSR circuit was chosen since it can be directly controllable through the data written to the shift register. For a specific clock frequency the data can be programmed in order to have switching activity level selectivity. Each LSR circuit occupies an area of 28 μm × 28 μm. The array structure of the LSR circuits occupy a total area of 672 μm × 896 μm. The LSR is of 32-bit length and capable of rotating its contents at 1 GHz frequency. Enabling and/or disabling the operation of each LSR provides the capability of controlling spatial and temporal correlations of the produced switching activity. The enabling/disabling of each LSR's operation (shifting their contents in loop mode with the externally adjustable clock speed) can be performed either independently, or row-wise or column-wise. The contents of the shift registers can be programmed randomly and independently while they are addressed. Similarly, they can be read back for testing purposes. If a write or read operation reaches the end of a file, in case of write operation, the new data written will overwrite the old in a cyclic manner, while in case of read, the data will be read all over again from the beginning of the file. This type of control was implemented on the LSRs by the means of SPI bus due to its simplicity and for minimizing the requried I/O pads/pins. The digital NT is depicted in Fig. 7. The silicon footprint of the noise transmitter is shown in Fig. 8(a).

4. Crosstalk noise sensing on a wireless communication SoC

The silicon prototype of the CMOS wireless communication – ZigBee application – SoC, fabricated in a 65 nm Low Power (LP) CMOS process, commercially available by TSMC, is shown in Fig. 8(a). Concerning the power consumption of the SoC, the particular ZigBee SoC appeared to be competitive with other available SoC ZigBee transceivers available either in the market or in the literature. In Table 2 this ZigBee transceiver power dissipation specifications versus the state of the art transceivers power specifications is depicted for the transmit (TX) and receive (RX) operation mode.

Two noise sensors were implemented for substrate noise sensing, the upper (noise sensor a in Fig. 8(a)) having the substrate input tap 2 μm and the down (noise sensor b in Fig. 8(a)) 10 μm away from the digital logic. A third one (noise sensor c) was also implemented as a standalone circuit just for performance characterization. The particular version had its input available externally

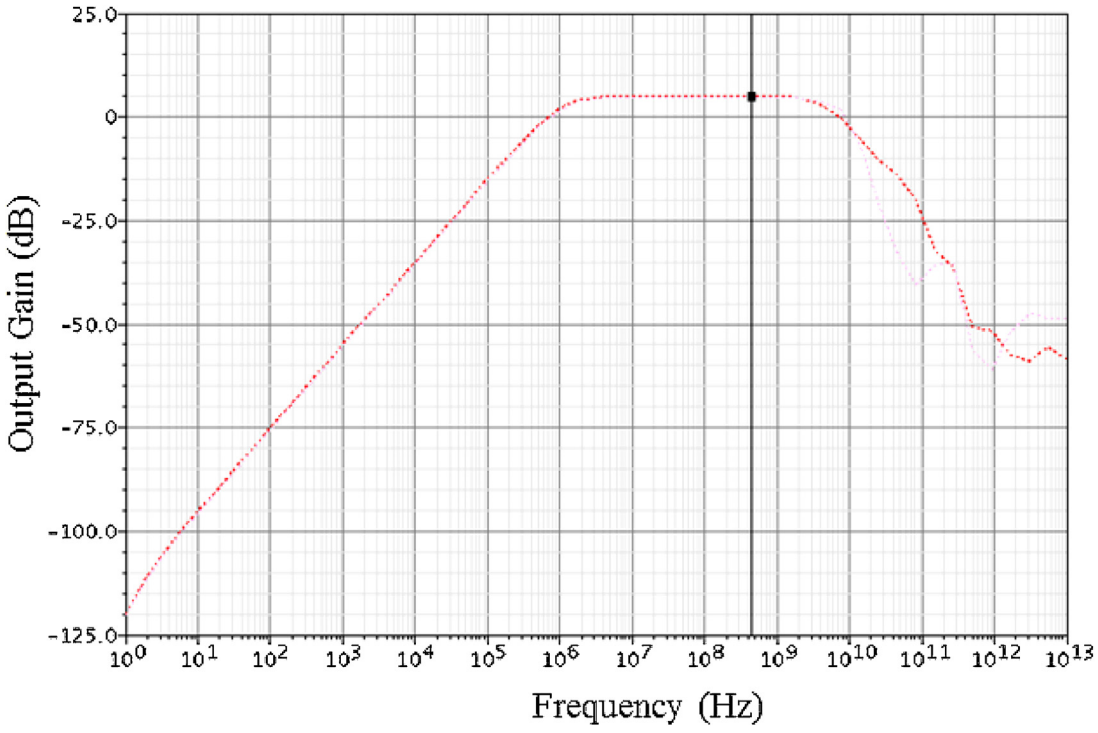

Fig. 5. Gain vs bandwidth (AC) simulation.

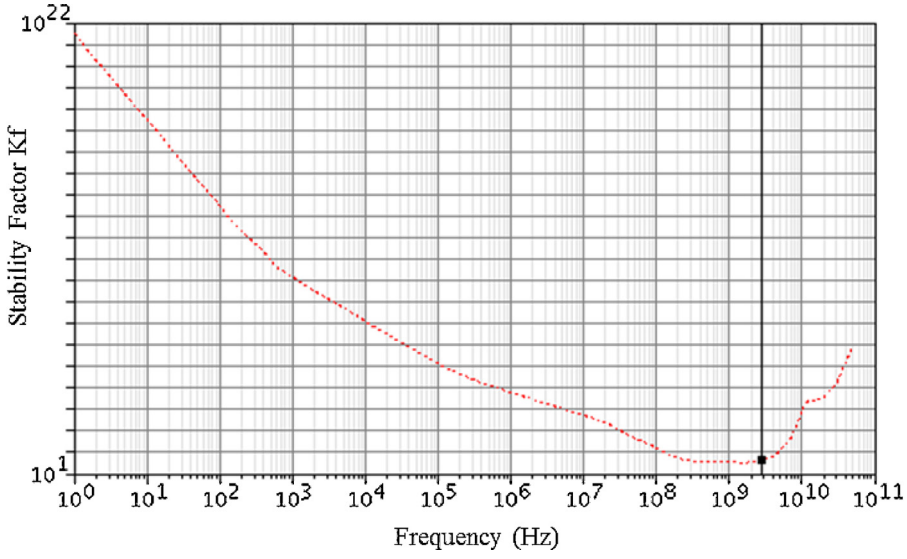

Fig. 6. Stability factor vs frequency (s-parameter) simulation.

Table 2
ZigBee transceiver power dissipation performance vs the state of the art.

	This work ZigBee transceiver	Ginés et al. [30]	TI [31] CC 2431	ATMEL [32] ATRF 230	Microchip [33] MRF 24J40	Freescale [34] MC 13193
V supply (*V*)	1.2	1.2	1.8	1.8	2.4	2.7
RX (mW)	43.0	31.0	48.6	28.8	43.2	113.4
TX (mW)	29.0	22.0	48.6	30.6	52.8	94.5

and a high frequency signal generator was used for the performance characterization. Since a Zigbee transceiver was implemented, several other RF circuitries are available onto silicon. Such as a low noise amplifier (LNA), a voltage control oscillator (VCO), a power amplifier (PA) (Fig. 8(a)), and several other peripheral blocks. The most sensitive one to substrate crosstalk noise was the LNA due to its close proximity to the digital control logic. The respective SoC PCB test board is shown in Fig. 8(b).

Concerning the substrate noise sensor standalone performance, sensor c was used for standalone characterization purposes. The

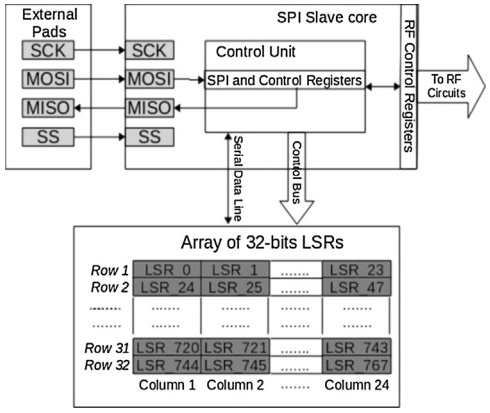

Fig. 7. Digital noise transmitter.

Table 3
Noise sensor performance characteristics.

Noise sensor characterization metrics	
Gain	6.5 dB
f-3 dB low	1.05 MHz
f-3 dB high	4.47 GHz
Vin_ampl@ −1 dB Compression point	124 mV

sensor provides a gain equal to 6.5 dB, in an operation bandwidth having low −3 dB frequency of 1.05 MHz and high −3 dB frequency of 4.47 GHz. The −1 dB gain compression point appears for input signal amplitude of 124 mV and the output *rms* noise voltage is equal to 129 μV. In Table 3, the noise sensor performance is summarized.

The proposed design appears as really advantageous and advanced compared to the state-of-the art available designs. An overall table containing all the available substrate crosstalk sensing techniques with respect to the design requirements is provided in Table 4. The proposed sensor is the only one that can operate in the high GHz region above 4 GHz, and at the same time satisfy all the rest design requirements. These are leaving unaffected noise propagation, being able to capture switching activity from the MHz region until the GHz region, being compact and area wise optimized and providing multiplexing capability for PIN number minimization. In addition, the upper −3 dB frequency can be really optimized to a much higher value in a lower technology node, and in a ball grid array package (BGA—Solder balls package) with much less inductive parasitics compared to the PGA approach.

The sensor's substrate noise capturing capabilities are depicted in Fig. 9. For both the noise sensors a and b, and in a frequency span from 100 MHz to 4 GHz, the measured noise spurs from the spectrum analyzer are provided having the 120 kGate digital logic with only the IO logic enabled and having both the IO and the Core logic fully enabled. All the crosstalk spurs captured with both the noise sensors at 2 μm and at 10 μm from the NT are given in Table 5. Only spurs with amplitude higher than −92 dBm are provided in Table 5. When the NT was fully disabled (IO and core logic 'OFF') both noise sensors did not capture any crosstalk spur with amplitude higher than −92 dBm.

The respective spectrum analyzer silicon measurements having disabled logic, IO logic 'ON' and core logic 'OFF' and both IO and core 'ON' are provided in Fig. 7 for both sensors.

From Table 5 and Fig. 9 it is extracted that noise sensor a, and exactly in the same frequency values as noise sensor b, captures noise signals of higher amplitude values, which is sanity wise correct since its substrate input tap is only 2 μm away from the digital logic instead of 10 μm of noise sensor b. In addition when full logic is 'ON' for both cases (2 μm and 10 μm away from the NT) the captured crosstalk spurs have higher amplitudes (on the same frequencies) compare to the lower switching activity case (only IO logic 'ON') which is also sanity wise correct. The related noise transmitter distance and gate switching activity level trends are depicted in Fig. 10, where the agreement of the substrate noise sensed signal trends to the general substrate coupling phenomenon performance behavior [13,17], are confirmed. The switching activity trend is presented for the sensor at 2 μm away from the NT (Fig. 10(b)).

Furthermore, the noise sensors can capture substrate noise signals with quite low amplitudes almost equal to −86.5 dBm that corresponds to 14.96 μV voltage peak amplitude, and also can capture really high amplitude signals in the range of 120 mV, achieving a quite satisfactory substrate signal sensing dynamic range considering the high frequency and broadband operating bandwidth.

5. Conclusion and future work

Substrate crosstalk sensing was performed in a 65 nm CMOS ZigBee wireless communication SoC. All the related crosstalk measurement requirements were addressed by implementing a novel CMOS architecture for sensing substrate noise signals. The particular architecture can sense directly substrate crosstalk noise signals in a wide frequency region from the MHz region until 4.5 GHz, and it is ideal both for wireless communication product level substrate coupling sensitive path detection and substrate crosstalk flow—noise integrity analysis validation. A detailed comparison with the state of the art crosstalk sensing techniques was performed, depicting the superiority of the proposed design. It appears as the most optimum and suitable to be used in wireless communi-

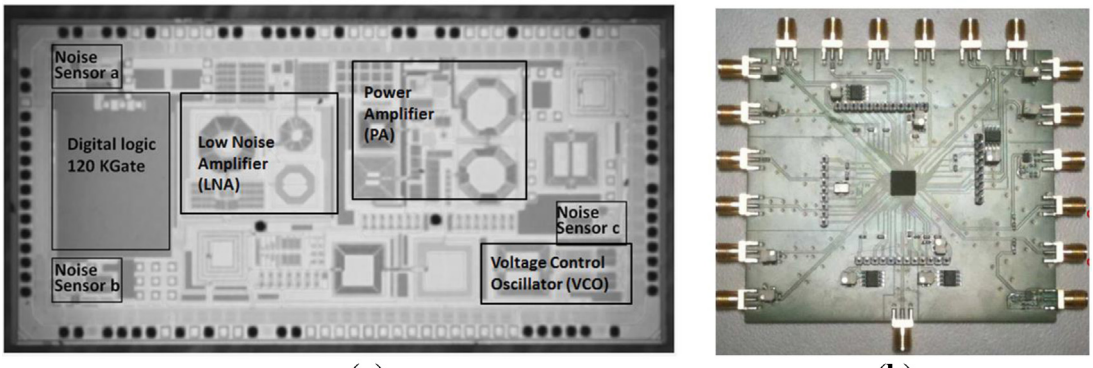

Fig. 8. (a) CMOS 65 nm wireless communication SoC Silicon footprint—noise sensors, digital logic noise transmitter and other RF components are highlighted (b) SoC PCB test board.

Table 4
Comparison of the proposed noise sensor to the available substrate noise sensing techniques.

Design specification	Sensor type					
	[18,19]	[20,21]	[22,23]	[24,25]	[26,27]	Proposed sensor
Do not affect noise propagation	√	×	√	√	×	√
GHz region upper frequency	×	×	×	×	×	√
MHz region low frequency	√	√	√	√	√	√
Compact and small size	√	×	√	√	√	√
Multiplexing capability	×	√	√	√	√	√

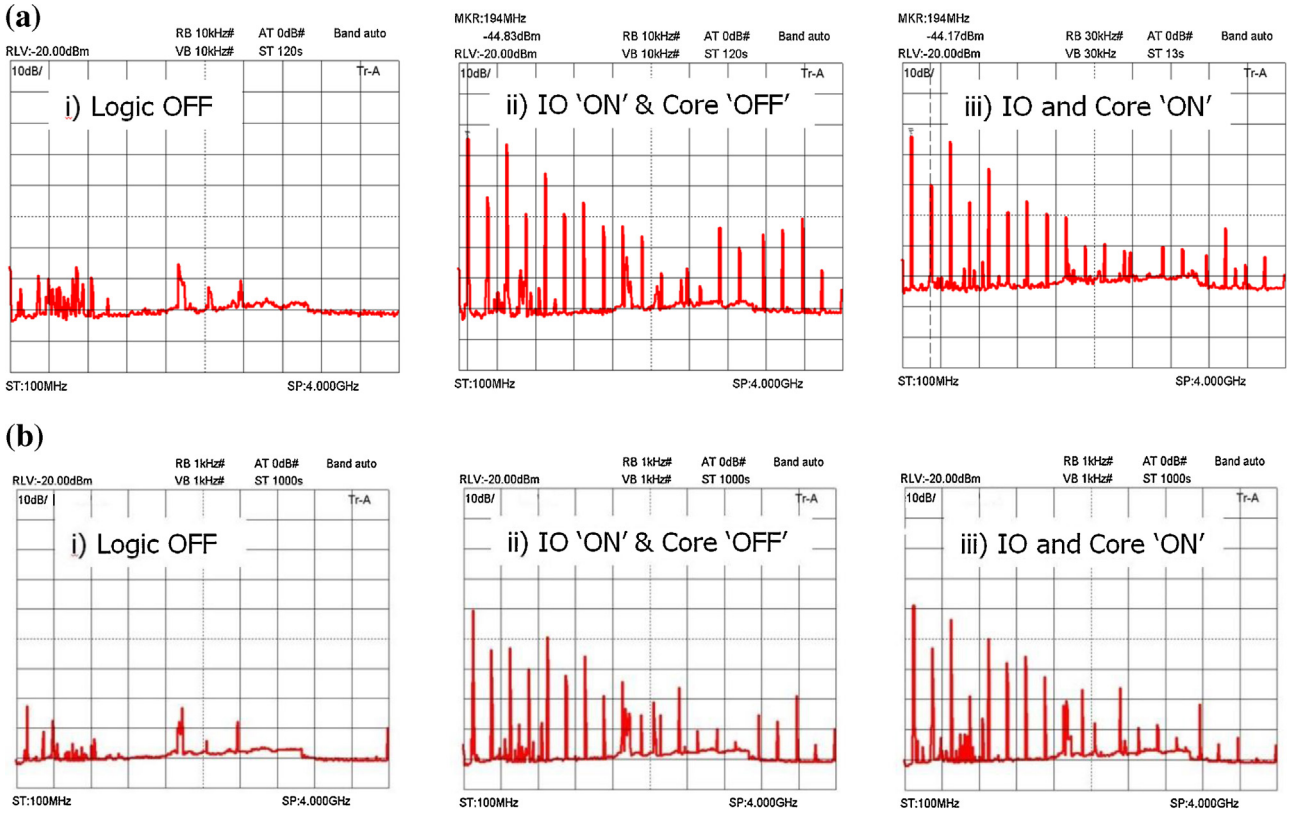

Fig. 9. Substrate noise signal capturing having the noise transmitter with different activity modes (a) at 2 μm away from the NT (b) at 10 μm away from the NT.

Table 5
Substrate noise captured signals with different enable and disable modes for the NT.

Substrate noise spurs—amplitude (dBm)				
Frequency(GHz)	Noise sensor at 2 μm from NT		Noise sensor at 10 μm from NT	
	IO 'ON' and core 'OFF'	IO and core 'ON'	IO 'ON' and core 'OFF'	IO and core 'ON'
0.194	−44.83	−44.17	–	−59.07
0.201	–	−44.33	−64.97	–
0.396	−63.95	–	−73.86	−73.17
0.591	−46.57	−46.05	−73.12	−63.96
0.786	−68.76	–	−89.14	−88.99
0.981	−56.94	−54.68	−69.99	−69.95
1.176	−69.17	–	−82.09	−78.72
1.371	−65.57	−65.47	–	−75.84
1.379	–	−65.74	−75.52	–
1.574	−73.21	−69.49	−88.86	−82.51
1.964	–	–	–	−86.73
1.769	−73.33	–	−84.34	–
2.362	–	–	−88.95	−86.37
3.392	–	−74.31	–	–
3.594	−70.92	−70.72	–	−86.41

cations SoCs for respective sensitive crosstalk paths identification and in general for real time substrate crosstalk measurements.

In terms of future work and addressing further improvements, and since the wireless communications are moving to higher frequencies and to the millimeter wave (5G) design era, higher

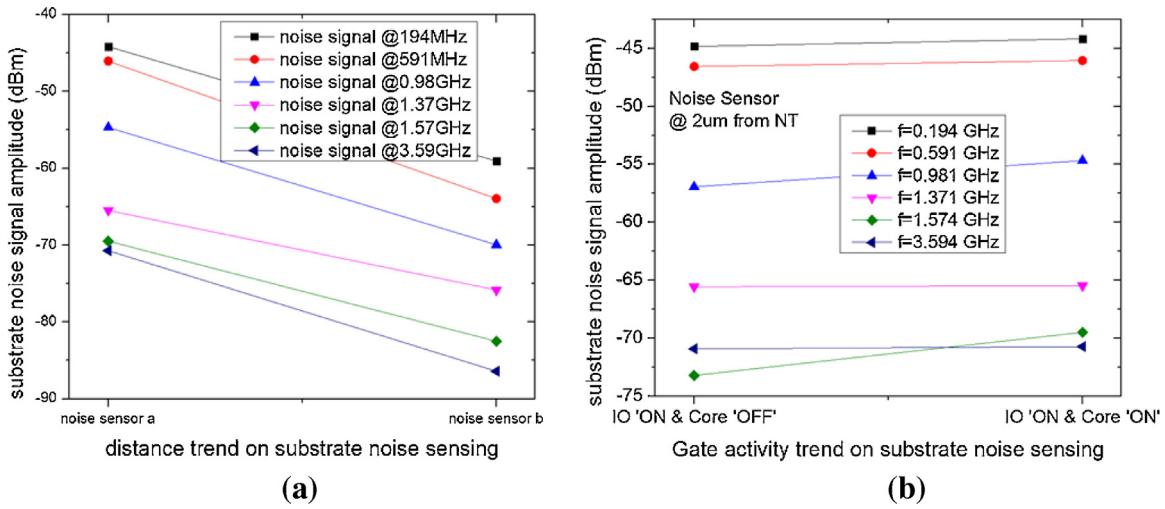

Fig. 10. Substrate noise sensing trends (noise amplitude) on (a) digital noise transmitter distance and (b) on switching activity level.

capacity will be required in sensing high frequency crosstalk signals and sensitive substrate crosstalk paths. Sensing substrate signals will be a need so as to separate magnetic crosstalk to substrate crosstalk. In addition, the imaginary part of the substrate impedance parasitics will be dominant in the emerging communications applications, imposing different mask level isolating techniques. There is also room for improvement in terms of the active silicon area, since optimized back end of line metal capacitors with higher metal density can be implemented and used. Also high performance electrostatic discharge (ESDs) structures with minimum active area can also be designed using compact structures.

Furthermore, based on the proposed design, and using a flip chip package and designing in a lower technology node, below 28 nm, with higher F_t (maximum unity current gain cut-off frequency) and F_{max} (maximum oscillation frequency) frequencies, a CMOS sensor that can reach even the 10 GHz operating frequency region can be implemented.

Concluding, the 5G communication era will require innovative circuit design in order to achieve a thorough silicon substrate signal sensing. Fabrication of compact SoC level noise sensors that can operate in decades of GHz frequency bandwidth and occupy really small active silicon area will be needed in product level real time testing for substrate crosstalk problems identification.

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