CMOS 65 nm 'on chip' broadband real time substrate noise measurement

T. Noulis✉, E. Lourandakis, S. Stefanou and P. Merakos

A CMOS 65 nm substrate crosstalk noise sensor with exceptional performance characteristics was implemented. The sensor is integrated and fabricated onto the same die with a pin-grid array packaged ZigBee transceiver. It provides a gain of 6.5 dB in an operating bandwidth from 1 MHz to 4.5 GHz and a −1 dB gain compression point for an input signal amplitude of 124 mV. Its superior substrate noise sensing capacity is demonstrated using measurements in an advanced wireless communication system on chip, having a programmable CMOS control logic of 120 kGate acting as the substrate noise transmitter.

Introduction: The wireless communication system on chip (SoC) contains cores of digital architectures integrated onto the same die with analogue/RF circuits. The significant performance improvement in terms of the speed and complexity of the digital circuitry results in an increase of generated digital switching noise. This noise is coupled through the common substrate (called substrate noise), with the sensitive analogue/RF circuits degrading their performance and resulting in product failures. Although many methodologies have been suggested to simulate the impact of digital switching noise on analogue/RF circuit performance [1, 2], even more challenging and crucial is to be able to validate if the substrate crosstalk noise simulation/flow is accurately correlating simulations with direct measured substrate noise signals and to identify critical substrate coupling paths. Substrate noise sensing techniques have been presented so far in [3–7]. None, however, provides capturing of substrate noise from the low MHz frequency region to the wireless communications GHz region and only Nagata [5] and van Heijningen *et. al.* [6] have implemented direct measurement circuitries. The main challenge is the really broadband gain behaviour needed to amplify the sensed substrate signals, and capture all the intermodulation's products in the wireless communication GHz region of interest and the direct substrate noise sensing feature needed so as to identify sensitive coupling paths.

In this Letter, a direct and broadband real time sensing topology is provided. Its operation is confirmed with silicon measurements on a CMOS 65 nm wireless communication pin-grid array (PGA) SoC, capturing substrate noise injected from a 120 kGate programmable IO and core digital logic, in a frequency range from a few MHz to 4.5 GHz.

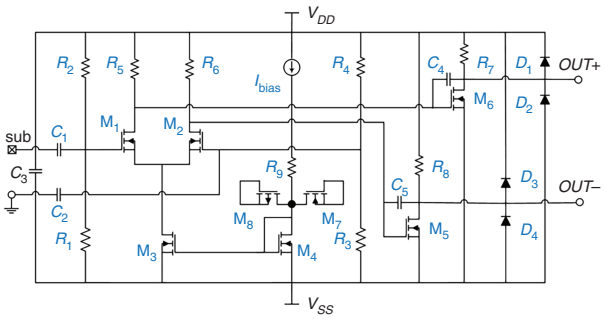

Fig. 1 *Substrate noise sensor schematic*

Substrate noise sensing: The noise sensor provided in Fig. 1 is a differential amplifier (1.2 V RF transistors M_1 and M_2) with one input connected to a dedicated quiet ground and the other connected onto substrate ('sub' in Fig. 1) so as to implement common mode rejection. Main objectives during the design have been a broad bandpass bandwidth (BW) response (from a few MHz to over 4 GHz) and the ability to deliver an output single ended signal to the 50 Ω load of a spectrum analyser. The back end of line metal capacitors C_1 and C_2 together with the resistor dividers R_1, R_2 and R_3, R_4 form highpass filters for the differential input. The resistance dividers also define the DC operating point of the differential pair. Resistors R_5, R_6 act as loads. The amplified substrate and the quiet ground reference signals are driven to M_5 and M_6. These open drain outputs (designed with thick gate 2.5 V devices) achieve the 50 Ω driving capabilities, lowering the output impedance and providing the necessary current to drive the 50 Ω instrument port. Low value capacitors C_4, C_5 are used to match the outputs *OUT* + and *OUT*− through the inductances of the SoC PGA package bond wires. R_7 and R_8 act as pull up resistors for the open drain outputs and M_8, M_9 and R_6 form an ESD protection for the input bias current and D_1, D_2 and D_3, D_4 for the differential RF output signals. The C_3 metal-insulator-metal decoupling capacitance is placed between V_{DD} and V_{SS} for supply ripple minimisation. A bias current of 750 µA and power supplies of $V_{DD} = 1.2$ V and $V_{SS} = 0$ V were used.

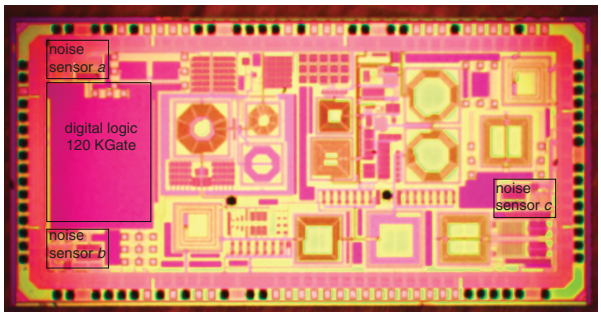

Fig. 2 *CMOS 65 nm wireless communication SoC silicon footprint – noise sensors and digital logic noise transmitter are highlighted*

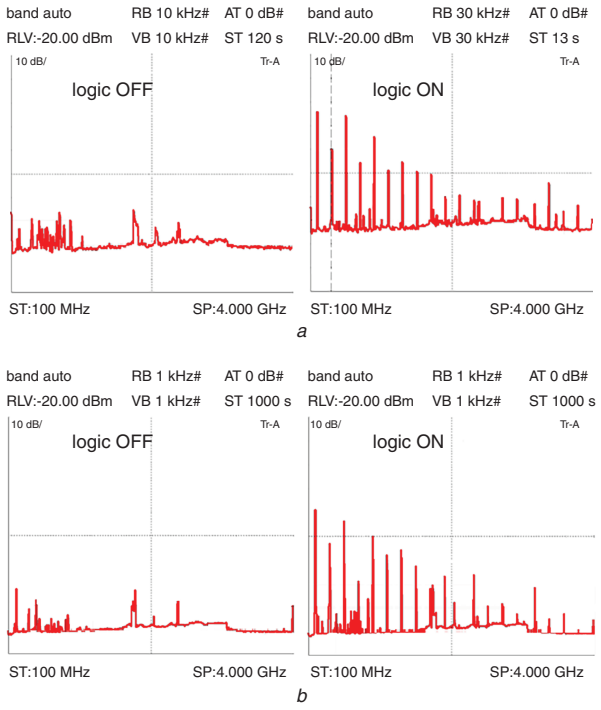

Fig. 3 *Substrate noise signal capturing having the noise transmitter enabled and disabled*

a Noise sensor *a* captured signals ('sub' tap 2 µm away from the logic)
b Noise sensor *b* captured signals ('sub' tap 10 µm away from the logic)

On the measurement aspect, an off-chip 5320B broadband transformer (balun), commercially available by Picosecond, was used (and simulated using an *S*-parameter model) for differential to single ended conversion. On chip routings parasitics, a PGA package and PCB board parasitics were extracted and simulated all in RLCk mode using a VeloceRaptor electromagnetic modelling engine [8] to capture all the performance high frequency effects and ensure silicon functionality.

The silicon prototype photograph of the CMOS wireless communication (ZigBee application) SoC, fabricated in a 65 nm low power CMOS process commercially available by TSMC, is shown in Fig. 2. Two noise sensors were implemented for substrate noise sensing, the upper (noise sensor *a* in Fig. 2) having the substrate input tap 2 µm and the down (noise sensor *b* in Fig. 2) 10 µm away from the digital logic. A third one (noise sensor *c*) was also implemented as a standalone circuit just for performance characterisation. The particular version had

his input available externally and a high frequency signal generator was used for the performance characterisation. The layout was fully symmetrical and special attention was paid in isolating sensitive devices using guard rings. The full sensor footprint lies onto a reversely biased deep *n*-well (*dnw*) and has an active area of 332 × 224 μm.

Table 1: Substrate noise captured signals having enabled digital logic

Frequency (GHz)	Noise sensor *a* output (dBm)	Noise sensor *b* output (dBm)
0.194	−44.17	−59.07
0.201	−44.33	—
0.396	—	−73.17
0.591	−46.05	−63.96
0.786	—	−88.99
0.981	−54.68	−69.95
1.176	—	−78.72
1.371	−65.47	−75.84
1.379	−65.74	—
1.574	−69.49	−82.51
1.964	—	−86.73
2.362	—	−86.37
3.392	−74.31	—
3.594	−70.72	−86.41

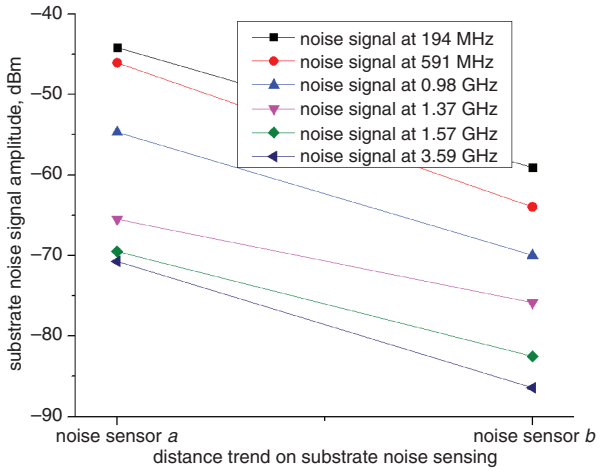

Fig. 4 *Substrate noise sensing trend (noise amplitude) on the digital noise transmitter distance*

The noise transmitter is a 120k Gate digital logic (1.2 V logic for the core and 2.5 V for the IO). This circuitry is a standard cell based design, acting as the control logic of the wireless SoC. On the noise activity, the logic consists of 768 loop shift registers (LSRs) arranged in 32 rows by 24 columns that are controlled and operated through a serial peripheral interface bus, defining high and externally adjustable switching activity. The LSR circuit has been chosen for the test chip and its switching activity is directly controllable through the data written to the shift register. For a specific clock frequency its data can be programmed to have a degree of selectivity on the produced switching activity. Each LSR circuit occupies an area of 28 × 28 μm. The array structure of the LSR circuits, occupy a total area of 672 × 896 μm. Enabling and/or disabling the operation of each LSR provided controlling the spatial and temporal correlations of the produced switching activity. The enabling/disabling of each LSR's operation (shifting their contents in loop mode with the externally adjustable clock speed) is performed independently, or row-wise/column-wise.

Concerning the substrate noise sensor standalone performance, the sensor provides a gain equal to 6.5 dB, in an operation BW having low −3 dB frequency of 1.05 MHz and a high −3 dB frequency of 4.5 GHz. The −1 dB gain compression point appears for a input signal amplitude of 124 mV and the output rms noise voltage is equal to 129 μV.

The sensor's substrate noise capturing capabilities are depicted in Fig. 3. For both noise sensors *a* and *b*, and in a frequency span from 100 MHz to 4 GHz, the spectrum analyser measured noise spurs are provided having the 120k Gate digital logic disabled and fully enabled.

The respective noise spur amplitudes captured in specific frequencies from the MHz region until 4 GHz are listed in Table 1. Noise sensor *a* captures noise signals of higher amplitudes compared with noise sensor *b*, which is sanity wise correct since its substrate input tap is only 2 μm away from the digital logic instead of the 10 μm of noise sensor *b*. The related noise transmitter distance trend is depicted in Fig. 4, where the agreement of the substrate noise sensed signal distance trend to the general substrate coupling phenomenon performance behaviour is confirmed [1, 2].

In addition, the noise sensor can capture substrate noise signals with quite low amplitudes almost equal to −86.5 dBm that corresponds to the 14.96 μV voltage peak amplitude and also can capture really high amplitude signals in the range of 120 mV, achieving a quite satisfactory substrate signal sensing dynamic range considering the high frequency broadband operating BW.

Conclusion: A novel CMOS architecture for sensing substrate noise signals has been implemented. The particular architecture senses directly substrate crosstalk noise in a wide frequency region until 4.5 GHz, and it is ideal both for wireless communication product level substrate coupling sensitive path detection and substrate crosstalk flow/noise integrity analysis validation.

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