



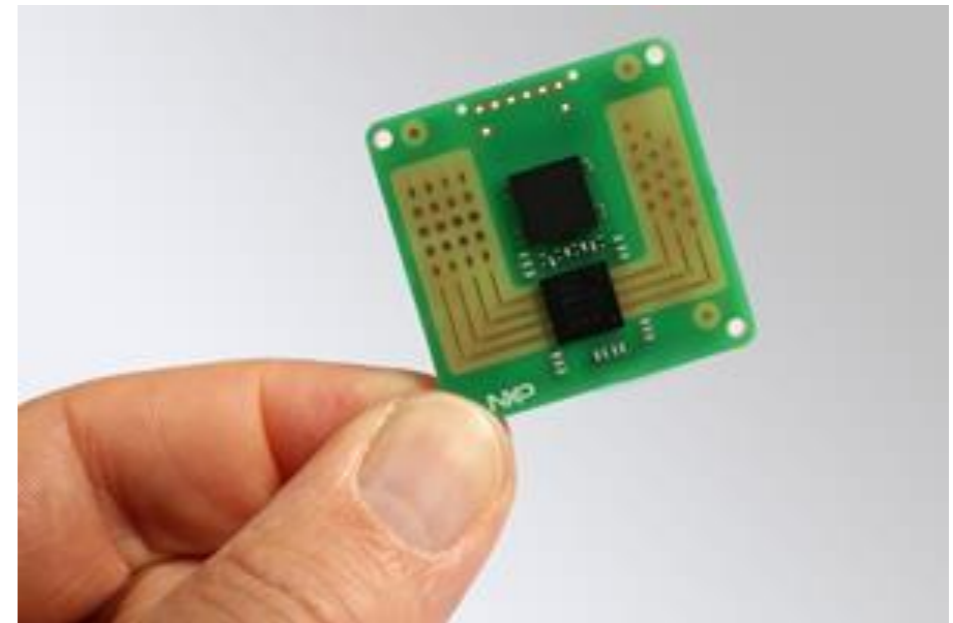
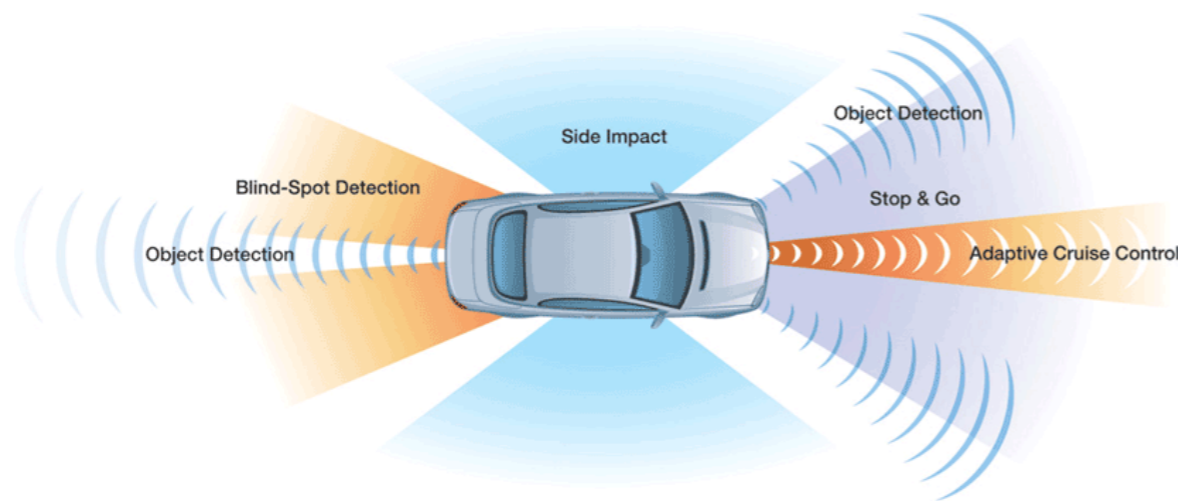
nm CMOS Device Synthesis for mm-Wave Design

Errikos Lourandakis
CDNLive Munich, May 2-4 2016

Why mm-wave silicon design?

- » nm CMOS mm-wave device synthesis
 - » Automotive radar 77-81GHz

Automotive Radar Applications



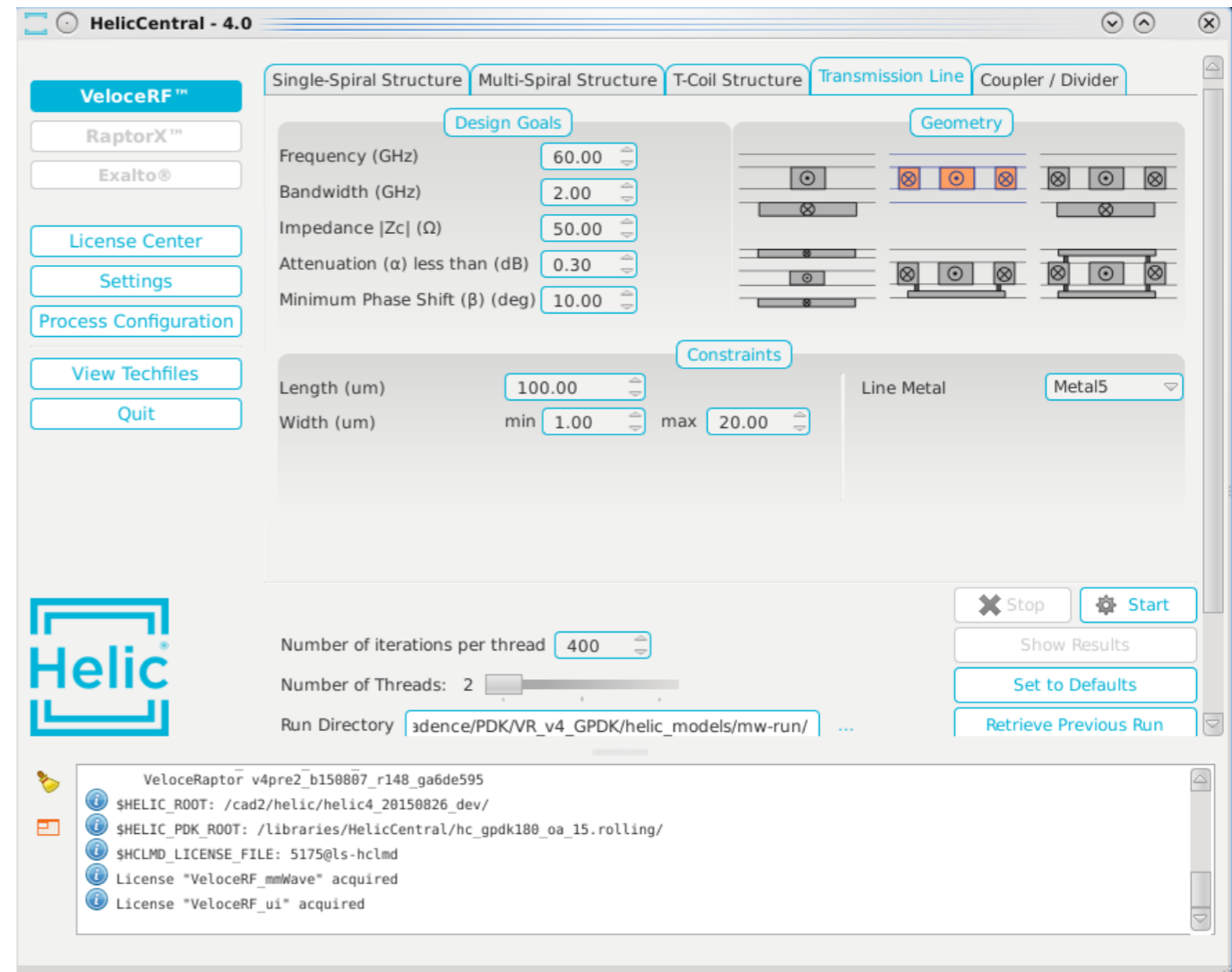
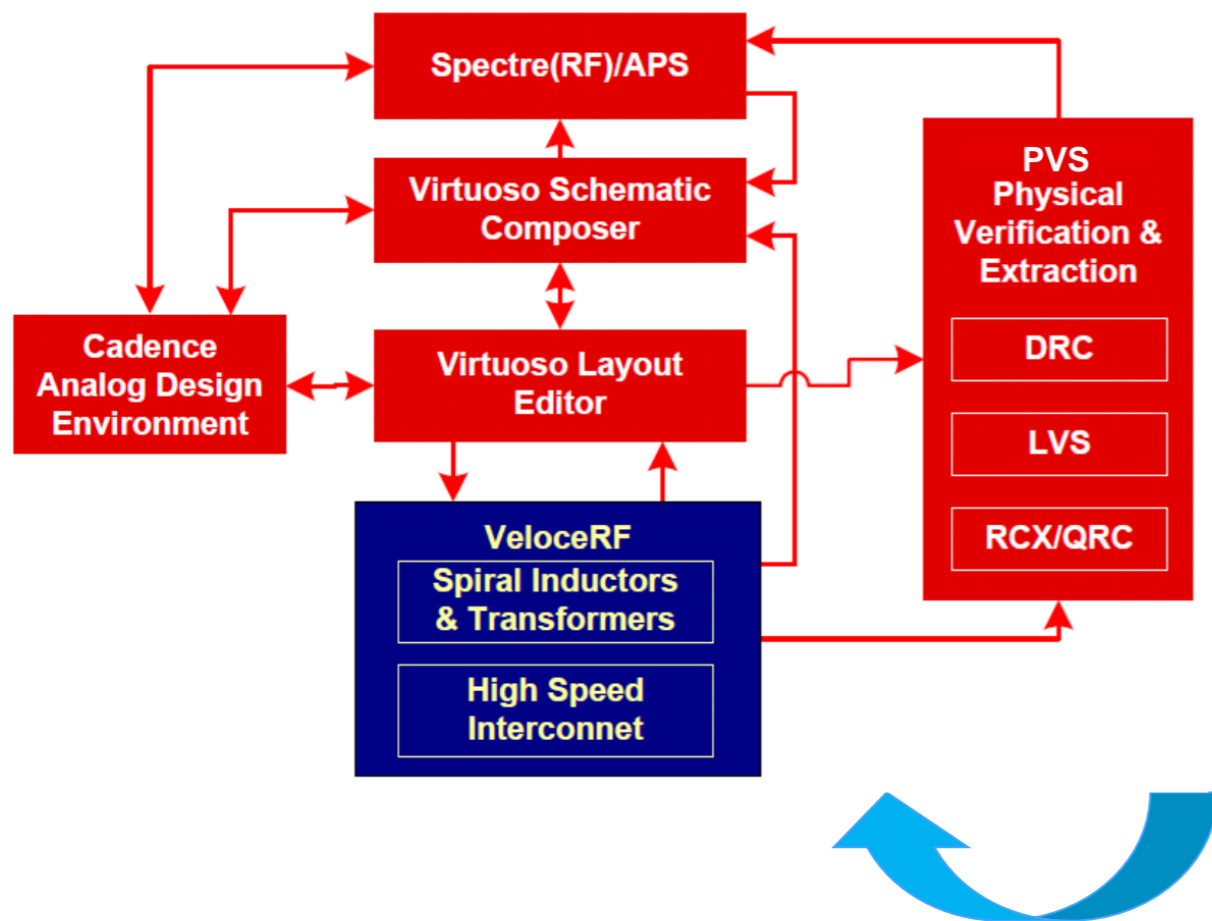
Source: NXP, CES 2016

- » Long range and short range radar around vehicle for advanced driver assistance systems (ADAS)
- » Existing solutions in SiGe and now CMOS
- » Demand for ADAS is massive ~ Millions of units/year

mm-wave silicon with Helic

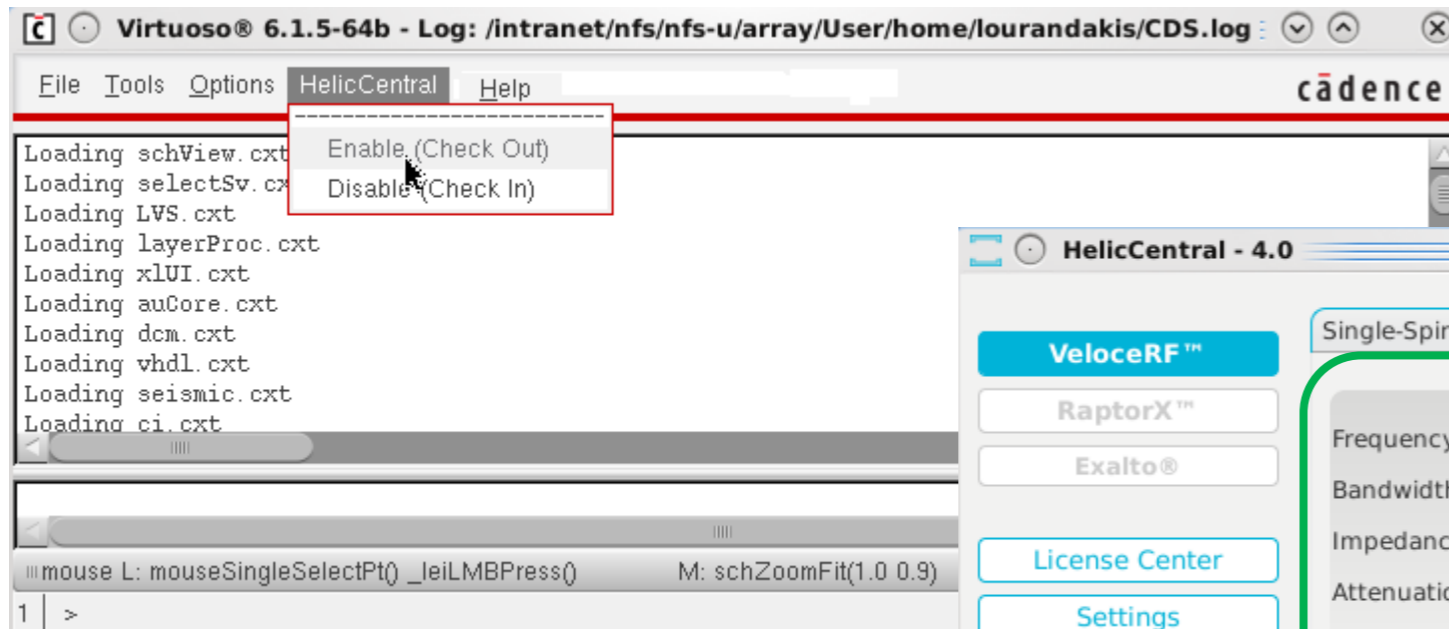
- » Helic's PCell synthesis inside Cadence Virtuoso
 - » mm-wave Transmission Lines, Bends, Junctions
 - » mm-wave Couplers
 - » DRC, LVS clean SKILL PCells
 - » Schematic and layout views for Cadence PVS flow
 - » RLCk and S-par models suitable for frequency and time domain analyses within Virtuoso ADE
 - » PCell synthesis down to 7nm/10nm/16nm CMOS

Where does Helic come into play?

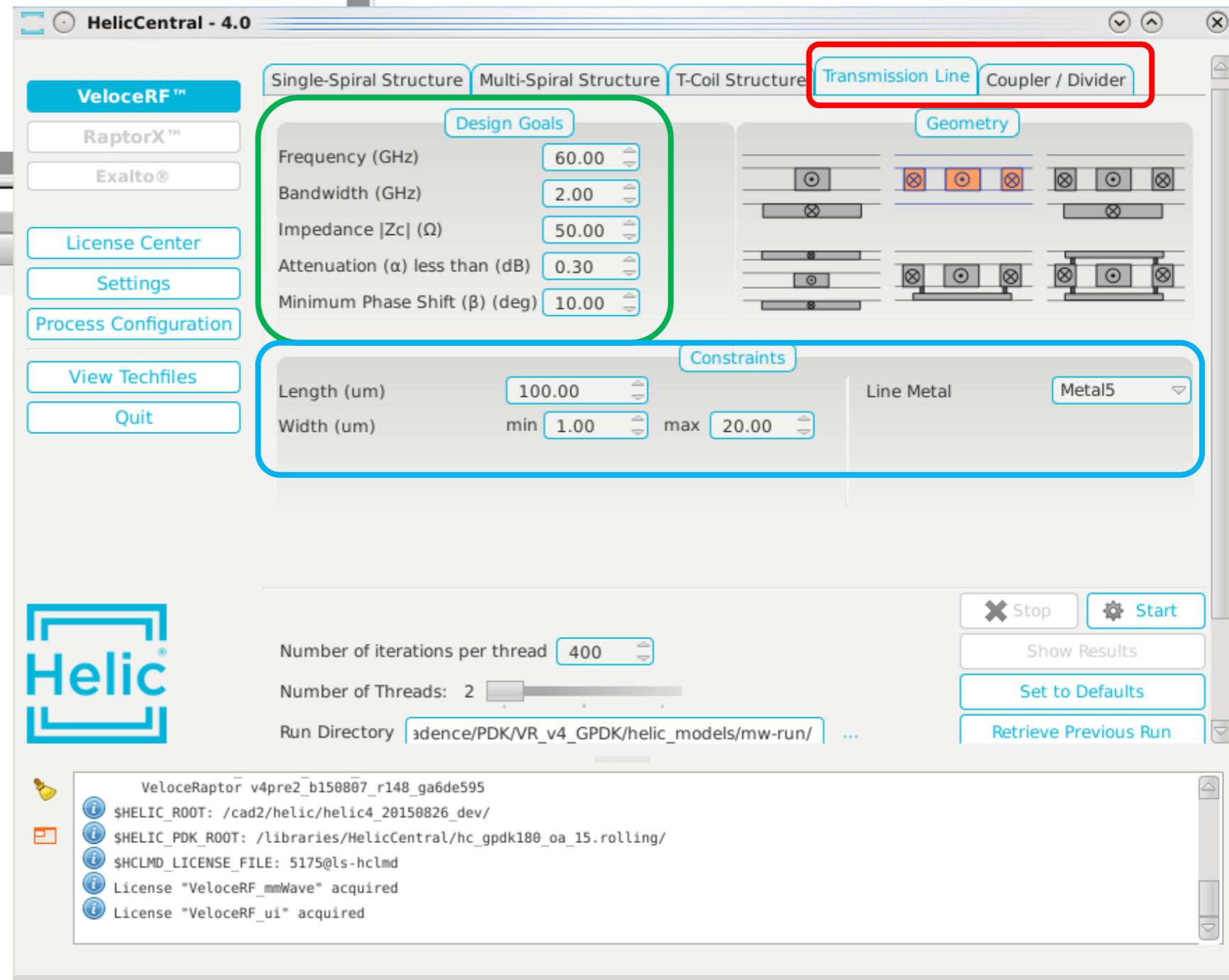


- mm-wave device synthesis integrated in Cadence
- Transmission lines, bends and couplers
- DRC, LVS clean PCells ready for mm-wave design

mm-wave Device Synthesis

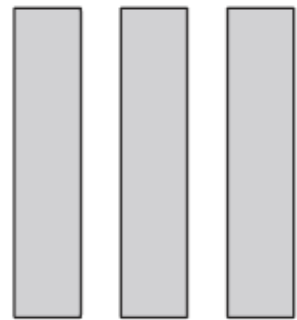


mm-wave PCells

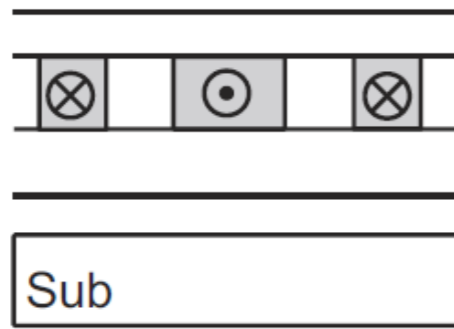


- » HelicCentral Suite seamlessly integrated in Cadence Virtuoso
- » VelocRF mm-wave
- » User defined constraint driven mm-wave device synthesis

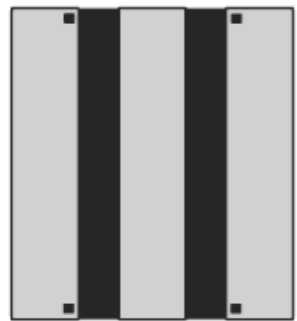
CMOS Transmission Lines



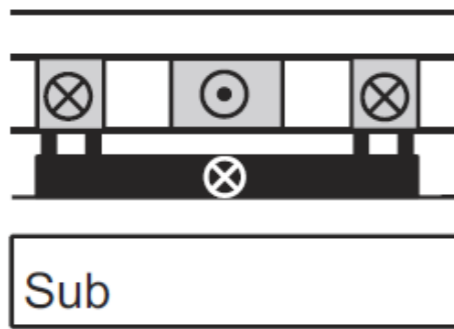
(a) CPW



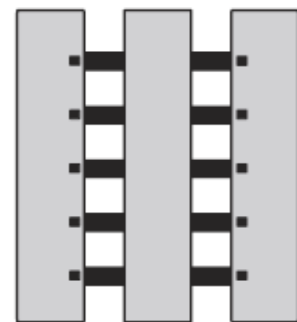
(b) CPW cross section



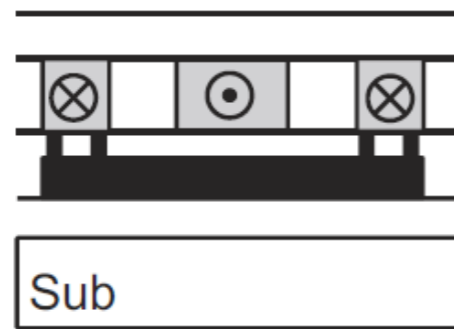
(c) CPWG



(d) CPWG cross section

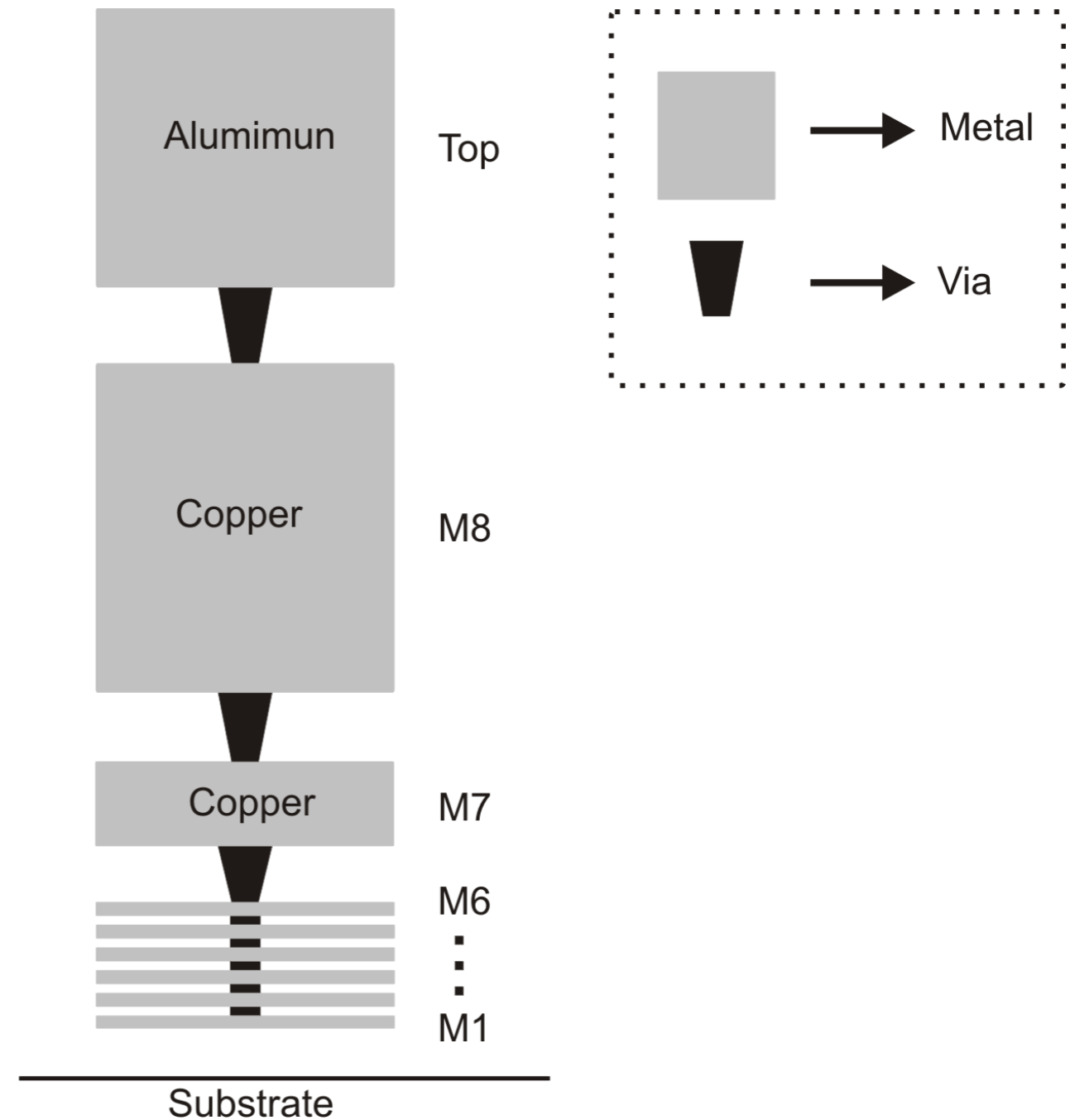


(e) SCPW

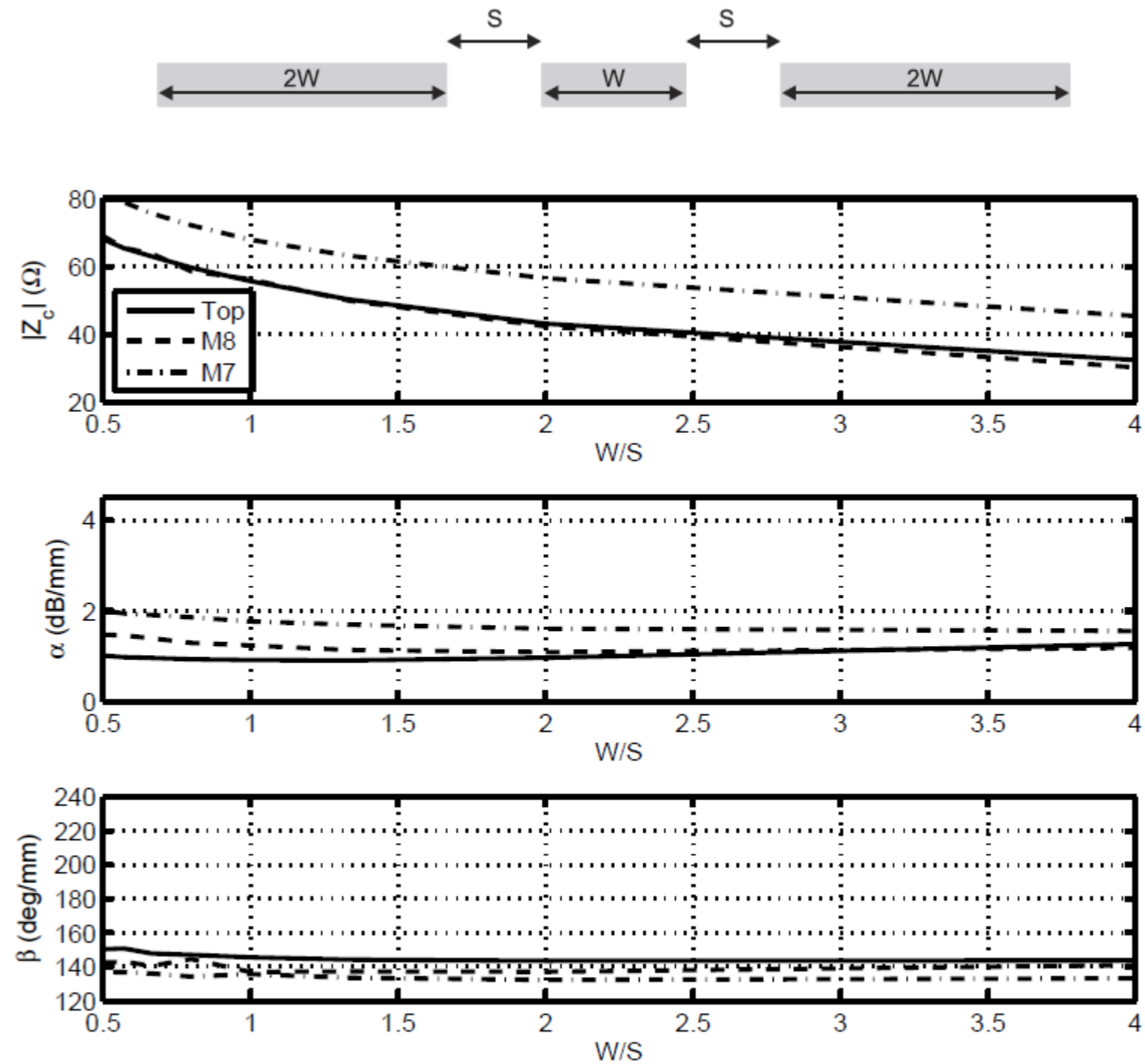
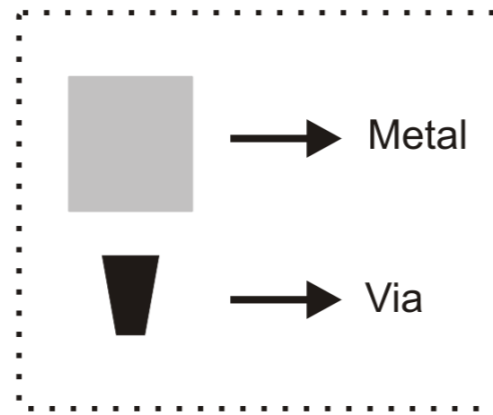
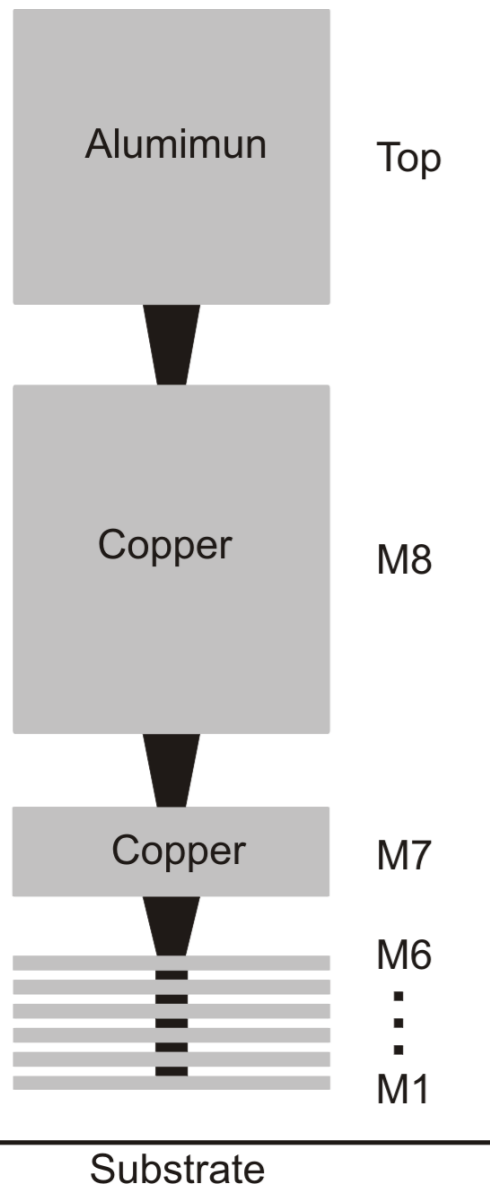


(f) SCPW cross section

Simplified 40nm CMOS BEOL



Where is the challenge?



➤ CPW T-line example

➤ Parametric analysis @ 60GHz

mm-wave T-line Synthesis

Design Goals

- Frequency (GHz): 60.00
- Bandwidth (GHz): 2.00
- Impedance |Zc| (Ω): 50.00
- Attenuation (α) less than (dB): 0.30
- Minimum Phase Shift (β) (deg): 10.00

Constraints

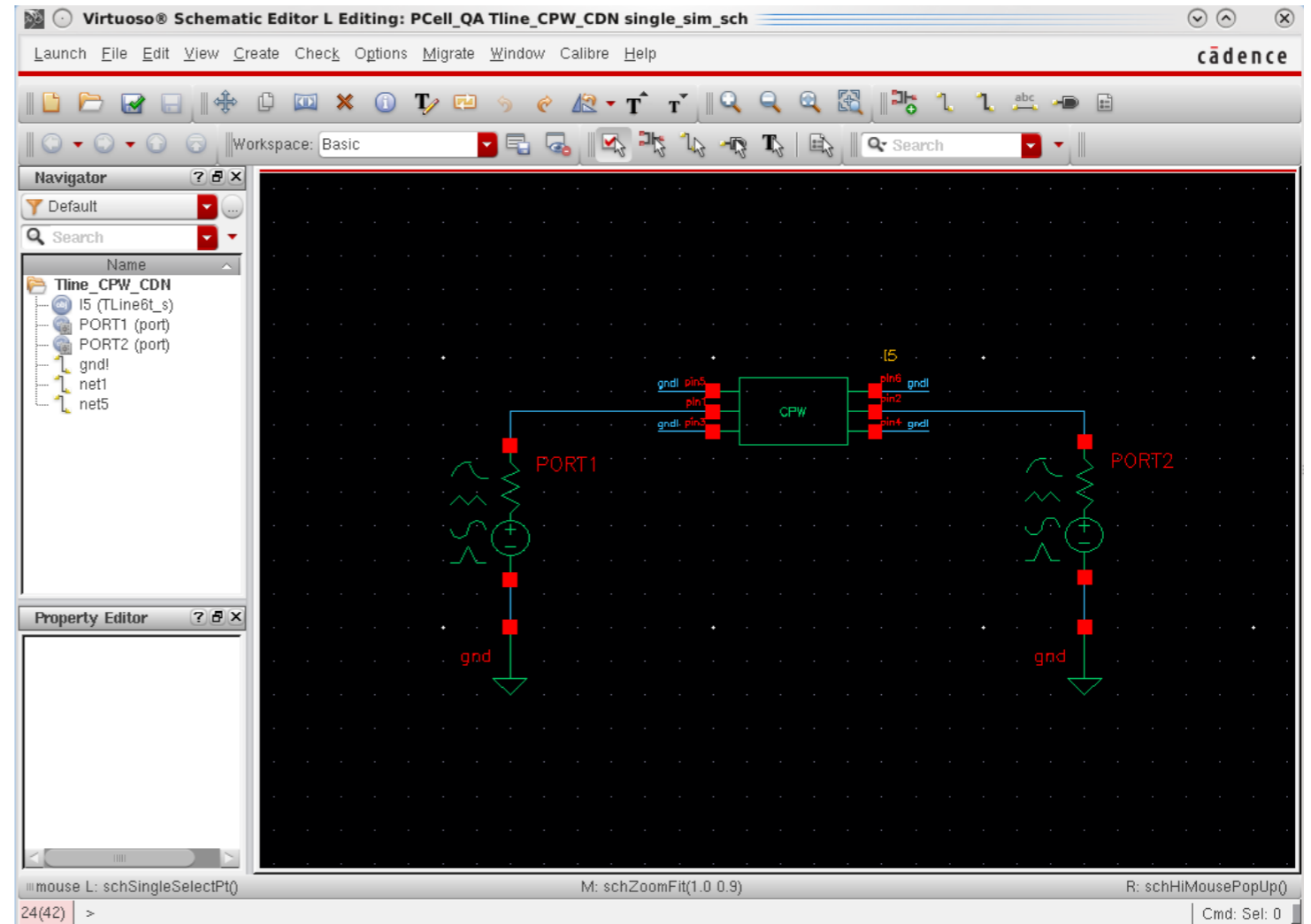
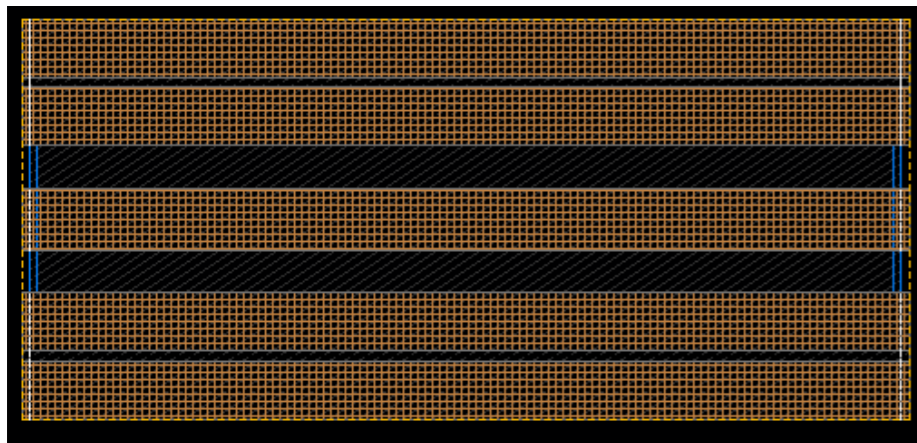
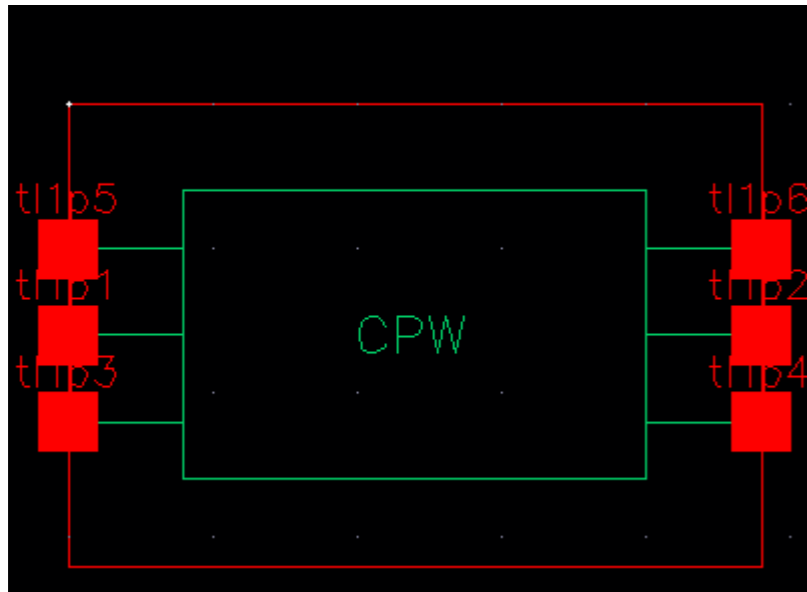
- Length (um): 100.00
- Width (um): min 1.00, max 20.00
- Line Metal: Metal5

Solutions

	F (GHz)	Zc (Ohm)	Z Low (Ohm)	Z High (Ohm)	Attenuation (dB)	Phase Shift (deg)	Length (um)	Width (um)
<input checked="" type="checkbox"/> Place	50	50.0748	50.0513	50.0985	0.258434	29.251	250	11.6
<input type="checkbox"/> Remove	50	50.0351	49.9971	50.0732	0.288849	29.2078	250	17.8
<input type="checkbox"/> Close	50	50.0558	50.0302	50.0814	0.262721	29.3584	250	12.4
	50	50.0141	49.9847	50.0435	0.267343	28.7718	250	14
	50	49.9897	49.9576	50.0219	0.273979	28.9144	250	15.2
	50	49.875	49.8368	49.9131	0.289657	29.2305	250	18
	50	51.5821	51.5411	51.625	0.2825	28.2258	250	18

- Synthesis returns multiple solutions matching user defined constraints
- Layout, schematic, and symbol views including RLCK model at your finger tips

Registered DFI views



- Automatically generated testbench
- Device model suitable for frequency and time domain analyses in ADE

PCell verification using Spectre

Virtuoso® Schematic Editor L Editing: PCell_QA Tline_CPW_CDN single_sim_sch

Launch File Edit View Create Check Options Migrate Window Calibre Help

Workspace: Basic

Navigator

- Tline_CPW_CDN
 - I5 (TLine6t_s)
 - PORT1 (port)
 - PORT2 (port)
 - gnd1
 - net1
 - net5

Property Editor

```

*** Copyright (C) 2000-2015 Helic, Inc.
*** Detailed model extracted by VeloceRaptor(TM) v4pre2_b151210_r294_g18822c1
*** @ Tue Jan 12 12:05:12 2016

*** Extraction Time: 5 sec
***
*** Modeler settings
***
*** Extraction temperature (if applicable)(Celsius): 27
***
*** Model reduced by NuRed(TM) v2.4_b151102_r3063_64
*** @ Tue Jan 12 12:05:31 2016
***
*** Reduction Bandwidth: DC - 110GHz
*** Ports Count: 6
*** Reduction Time: 14 sec
***
*** Reduction Statistics:
***      Input      Output
*** Elements Count: 2915146 --> 8155
*** Nodes Count:   3733 --> 820

simulator lang=spectre

subckt Tline_CPW_CDN ( hc1_pin1 hc1_pin2 hc1_pin3 hc1_pin4 hc1_pin5 hc1_pin6 )

R0_0 (0 n7) resistor r=10.00000001569897
C0_0 (0 n7) capacitor c=1.7916604782119777e-12
C_0_1 (n7 n8) capacitor c=-3.32498265940821e-16
C_0_2 (n7 n9) capacitor c=2.448617966356255e-16
C_0_3 (n7 n10) capacitor c=-2.659619370021091e-17
C_0_4 (n7 n11) capacitor c=2.745653603441261e-15
C_0_5 (n7 n12) capacitor c=-1.766302606152624e-12
C_0_6 (n7 n13) capacitor c=2.693654909827702e-13
C_0_7 (n7 n14) capacitor c=-2.969750766344274e-14
C_0_8 (n7 n15) capacitor c=-8.762459751872612e-19
C_0_9 (n7 n16) capacitor c=4.932397373171771e-19
C_0_10 (n7 n17) capacitor c=-2.99769696910156e-18
C_0_11 (n7 n18) capacitor c=4.011038439963249e-18
C_0_12 (n7 n19) capacitor c=2.456504709193734e-18
C_0_13 (n7 n20) capacitor c=-3.724025573261719e-19
C_0_14 (n7 n21) capacitor c=-5.354139736885057e-18
C_0_15 (n7 n22) capacitor c=5.765859973706057e-18
C_0_16 (n7 n23) capacitor c=3.325608724784772e-17
C_0_17 (n7 n24) capacitor c=2.633153066490085e-18
    
```

Virtuoso® Analog Design Environment (3) - PCell_QA Tline_CPW_CDN single_sim

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Helic Help cadence

27

Design Variables

Name	Value

Analyses

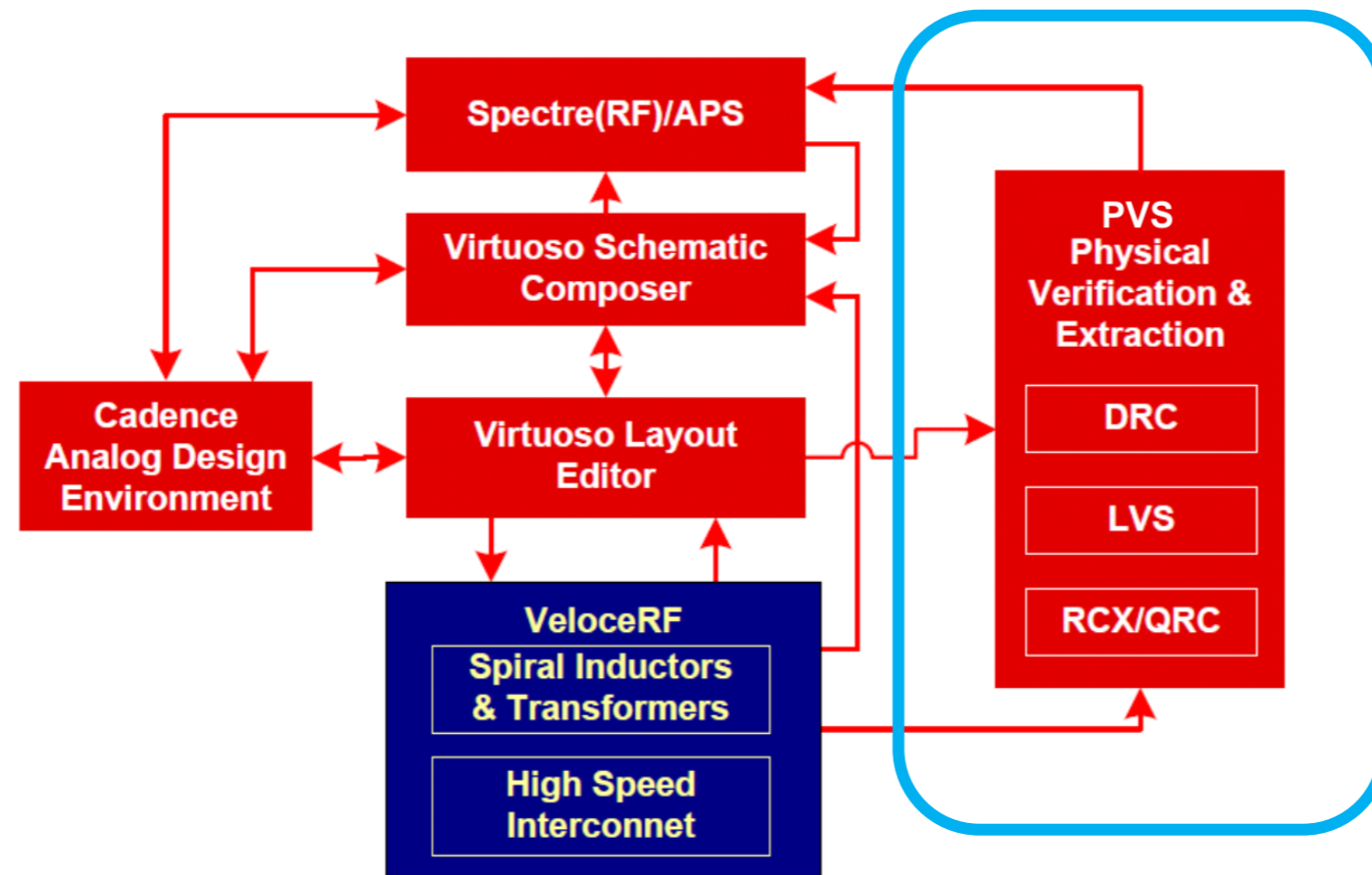
Type	Enable	Arguments
sp	<input checked="" type="checkbox"/>	100M 110G 100M Linear Step Size Start-Stop

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options

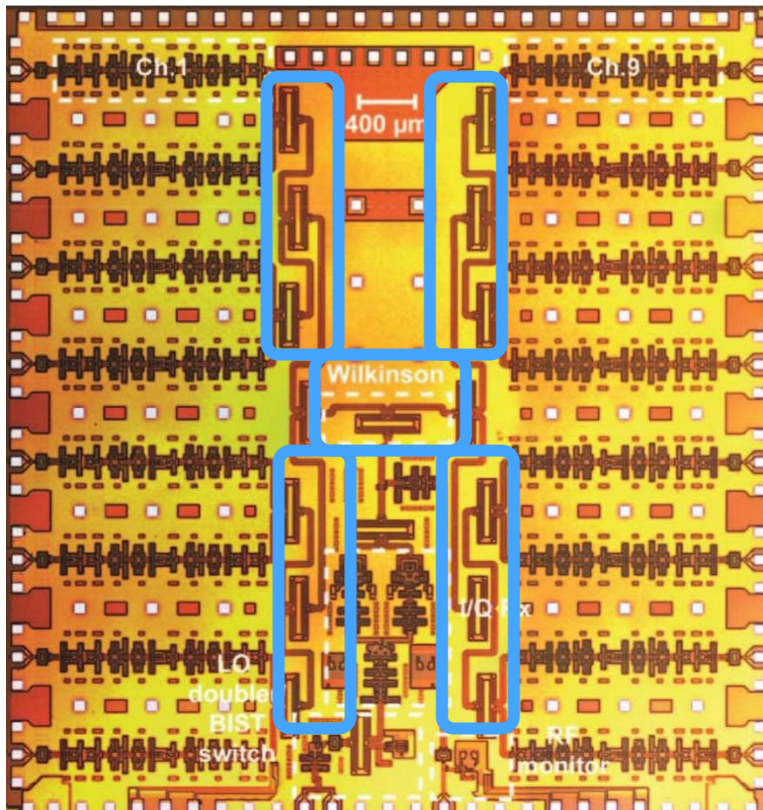


Integration to Physical Verification

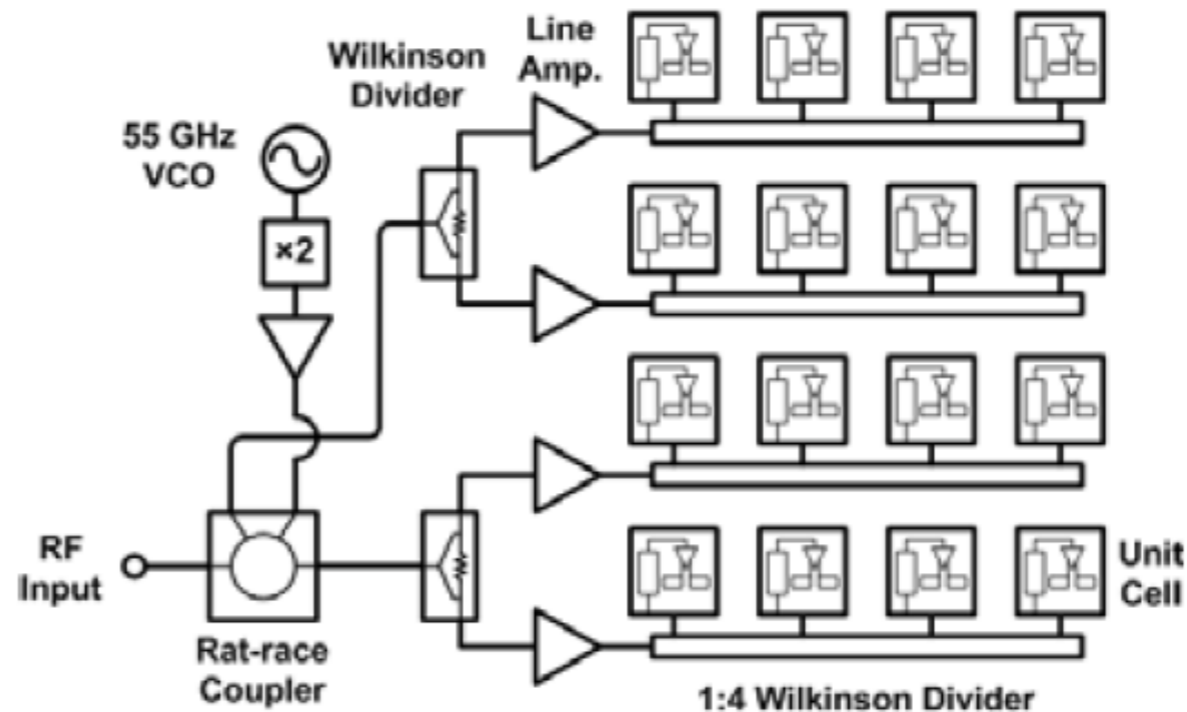


- » PCell inserted in top-level layout
- » User runs PVS DRC, LVS as usual in top-level layout
- » Quantus QRC invoked from layout for extracting parasitic components of entire circuit

Are mm-wave passives relevant?



Source: UC San Diego, IEEE 2015
Multi-channel 77-81GHz SiGe radar



Source: UC San Diego, IEEE 2015
110 GHz Transmit Phased Array Topology

- T-lines and mm-wave couplers (e.g. Wilkinson divider) are key building blocks
- Physics for nm CMOS design are complex
- Automated and constraint driven design is needed

Helic's unique mm-wave flow

» Example 1

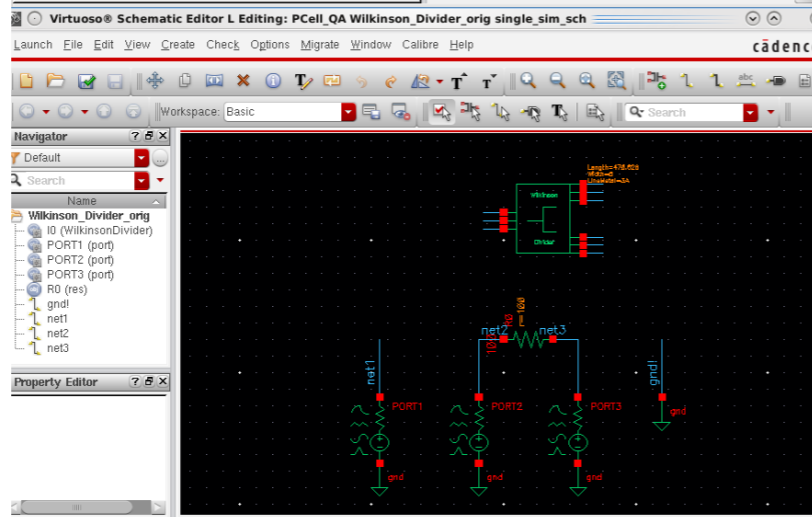
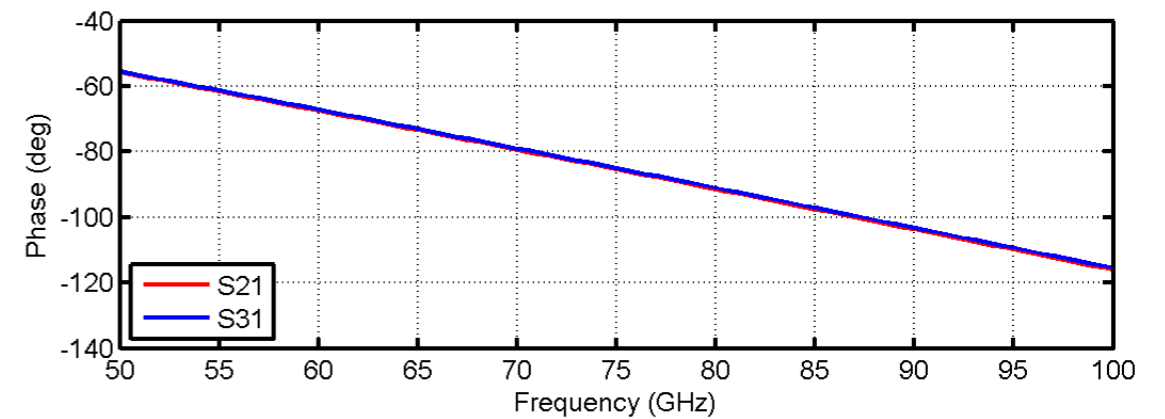
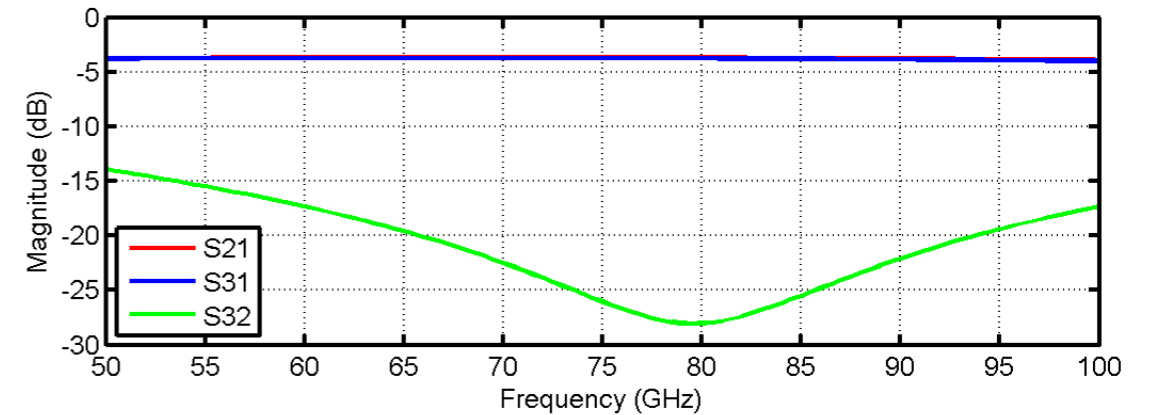
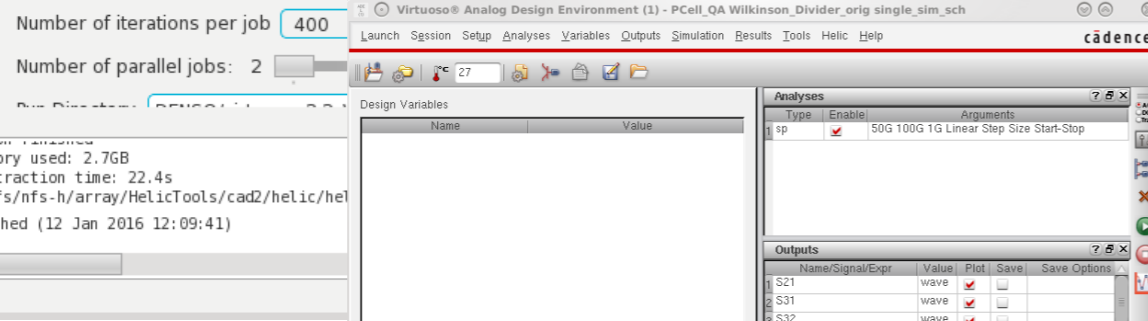
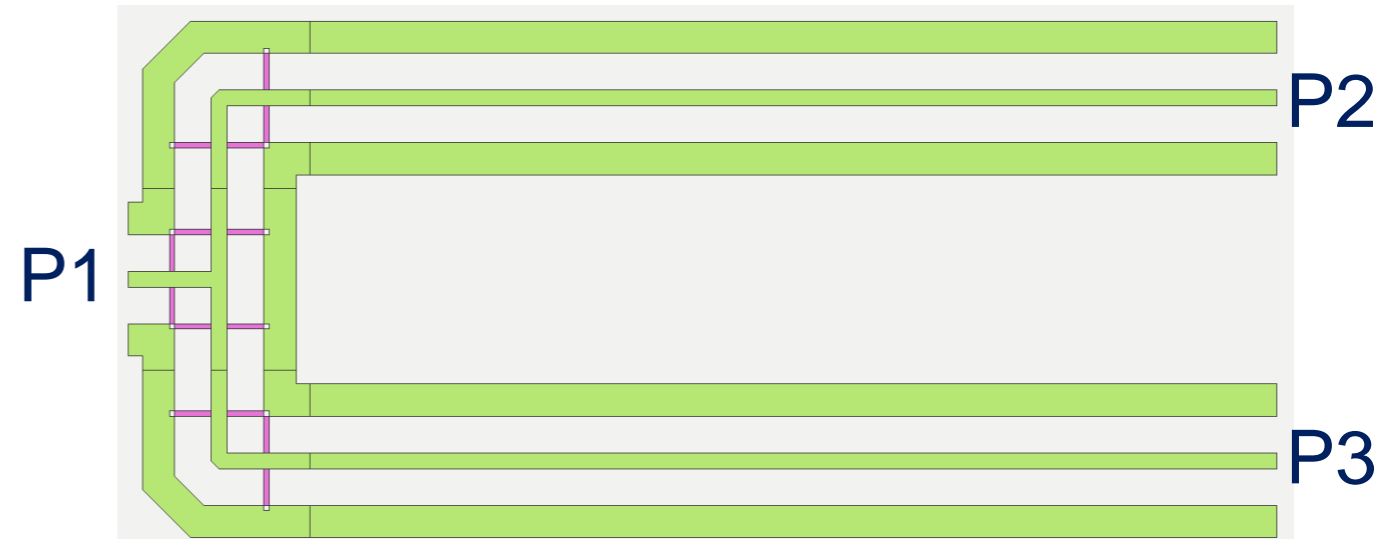
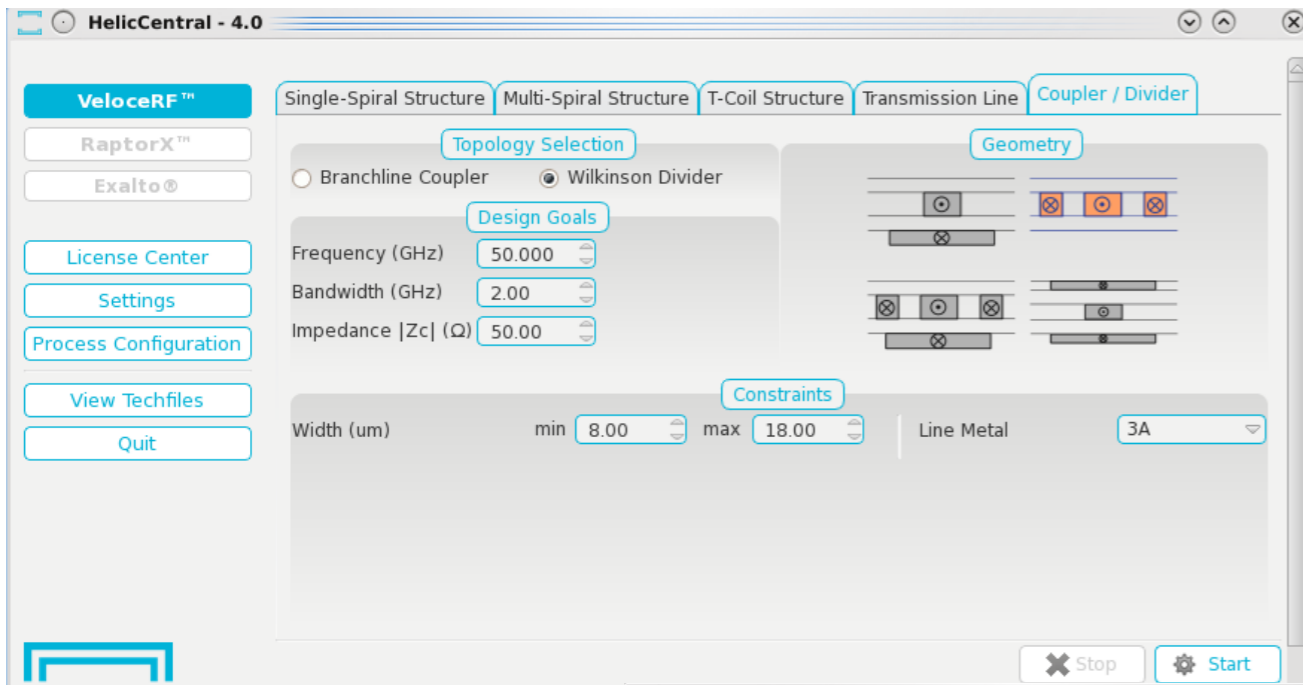
- » Synthesis of Wilkinson divider by VeloceRF
- » 77-81GHz tuned divider
- » Fully customizable PCell in Cadence (DRC, LVS, PVS compliant)

» Example 2

- » Custom Wilkinson divider design based on Helic's mm-wave PCells (T-lines, Bends and Junctions)
- » 77-81GHz tuned divider
- » Custom device for Cadence verification flow

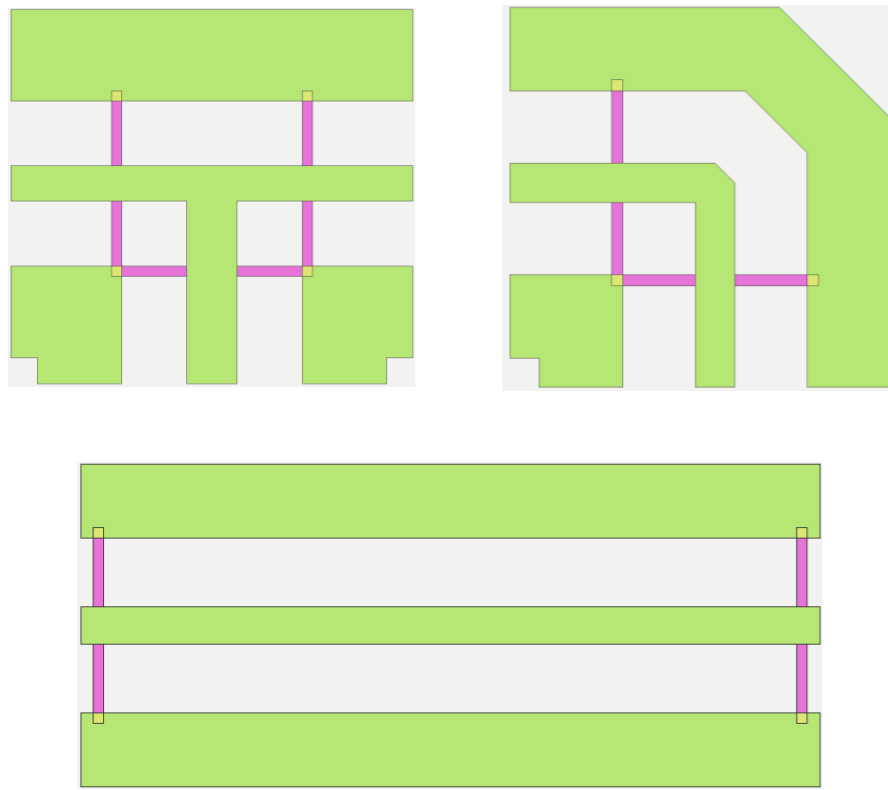
Example 1 – Divider PCell

Area: 0.0871mm²

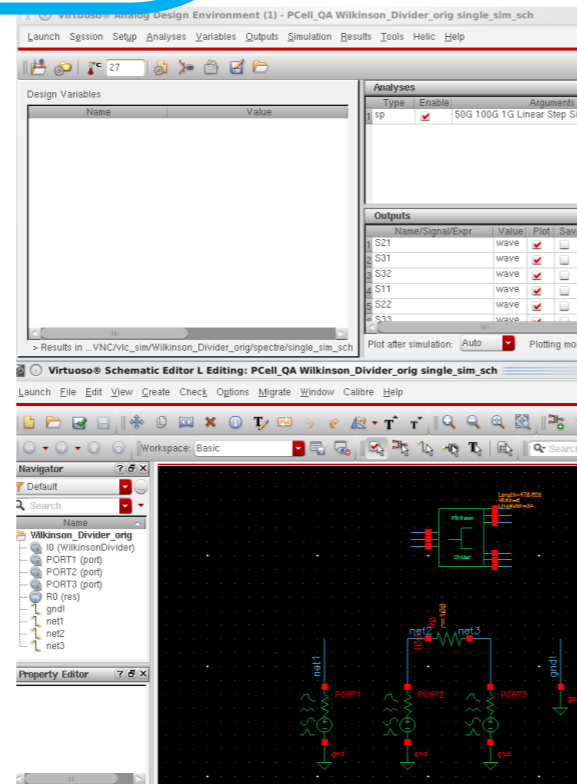
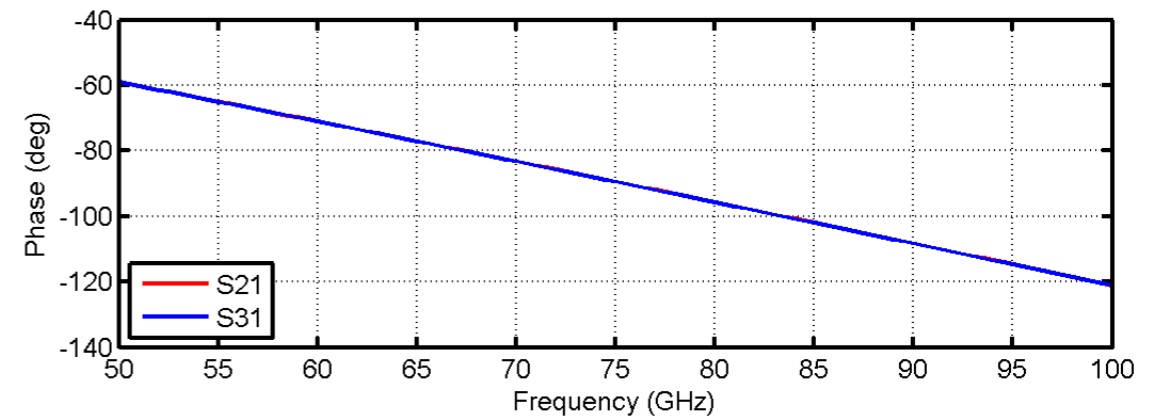
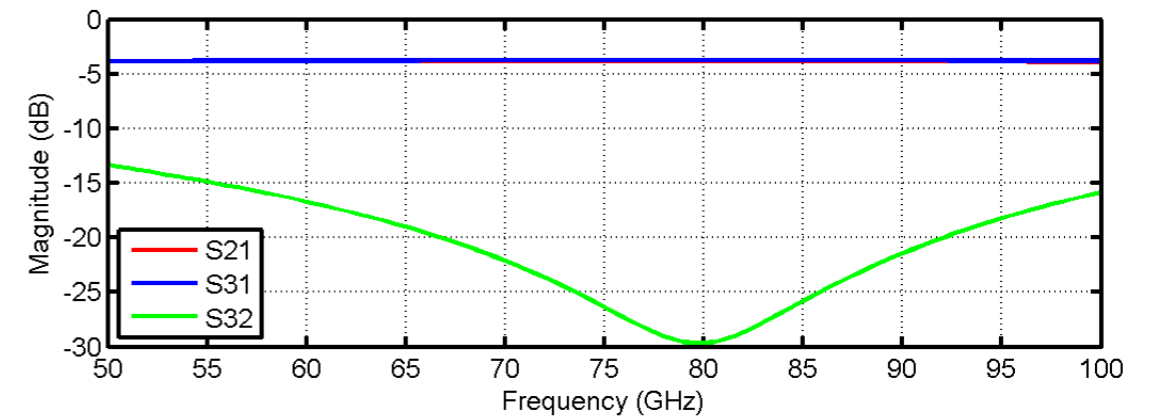
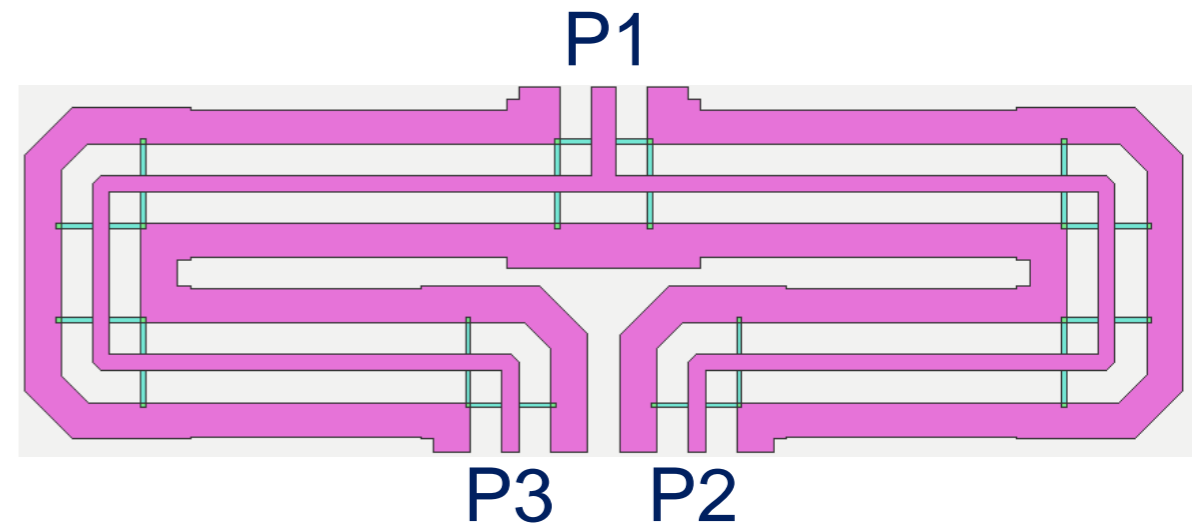


- » Automated and faster synthesis
- » Schematic / Layout view
- » Simulate device in ADE

Example 2 – Custom Design

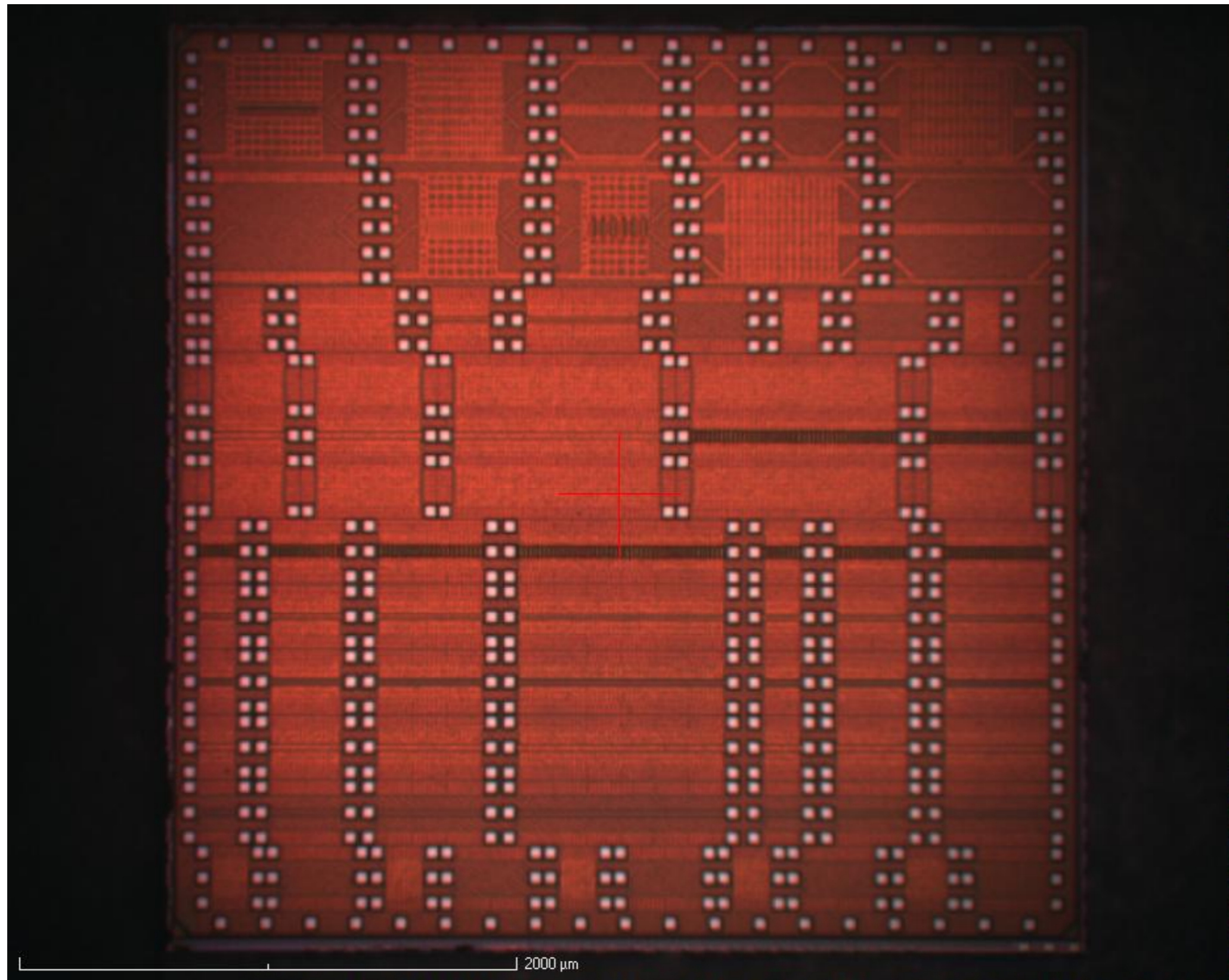


Area: 0.0744mm²



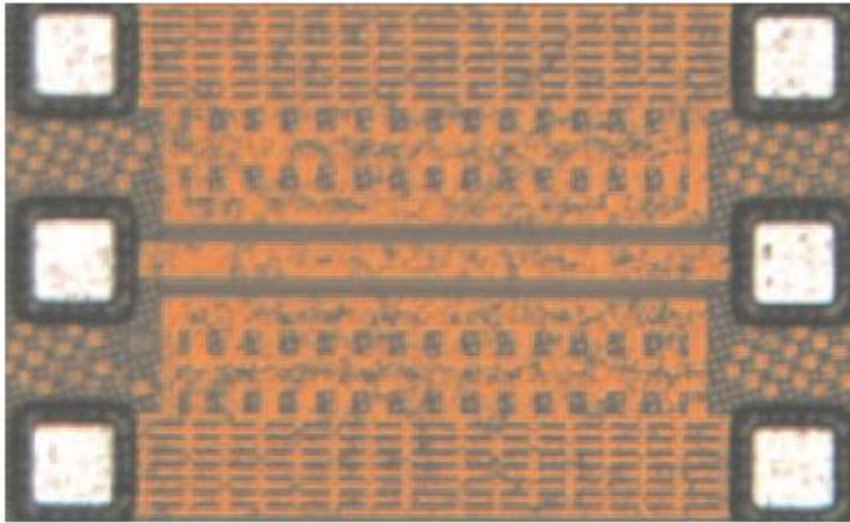
- » PCells used for area optimized design
- » Smaller footprint
- » Custom Device

mm-wave 40nm CMOS test chip

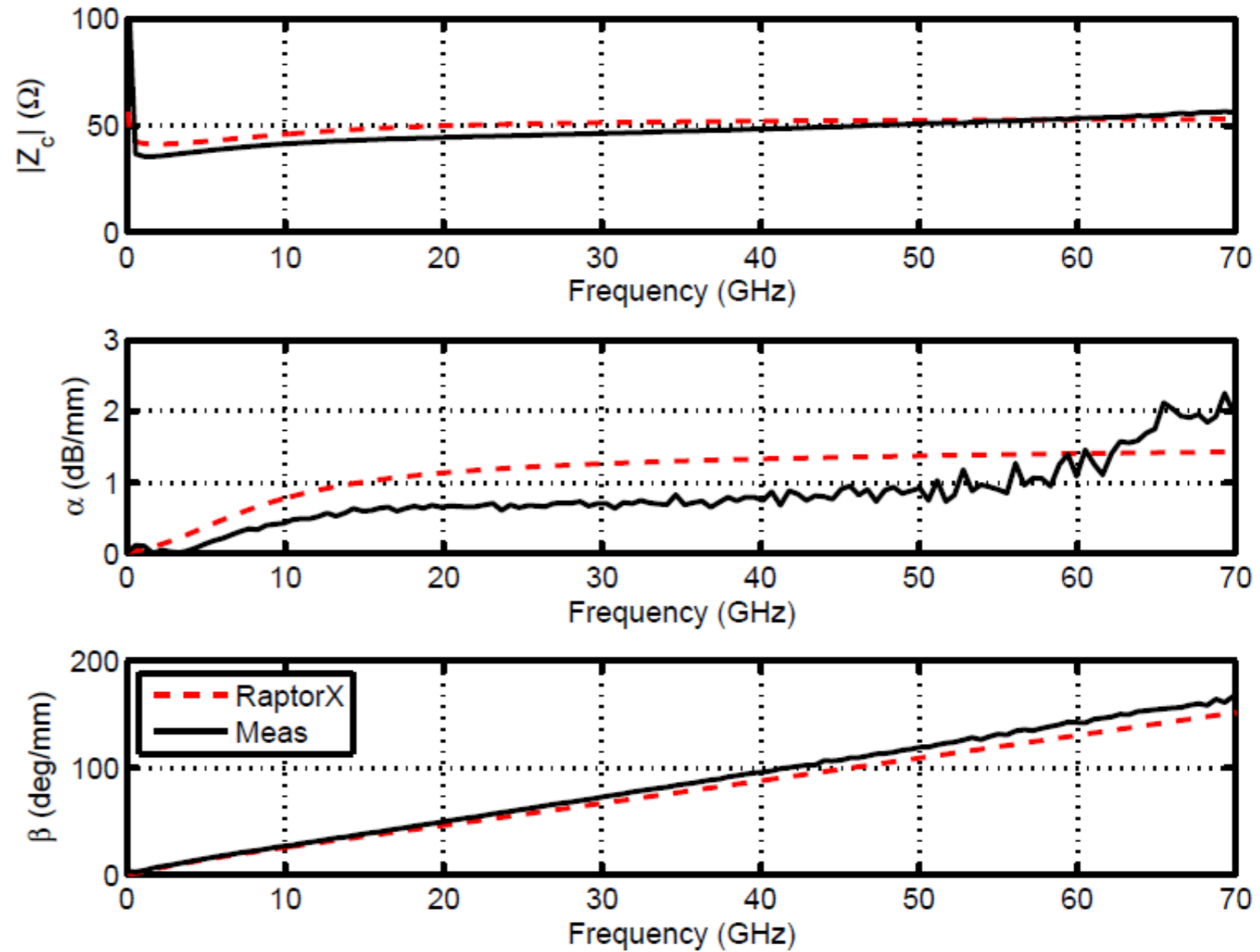


mm-wave Silicon – CPW

➤ CPW T-line

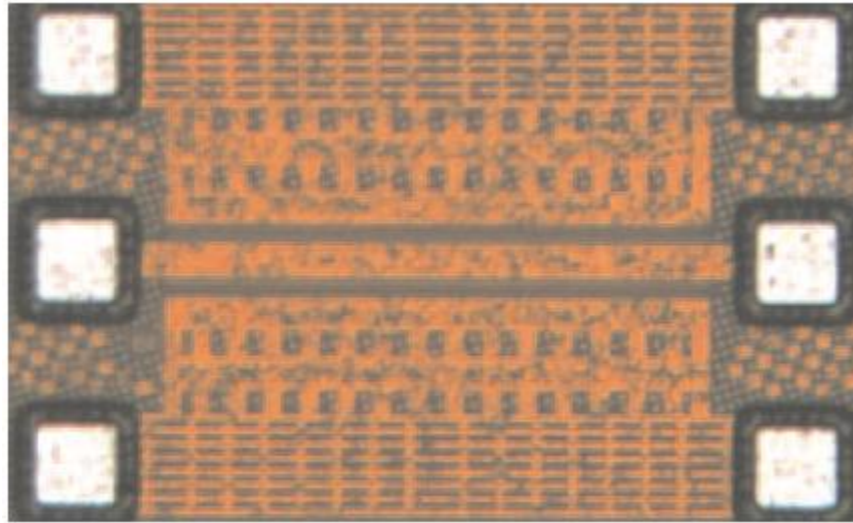


$$Z_c = \sqrt{\frac{B}{C}}$$
$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A))$$
$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A))$$



mm-wave Silicon – SCPW

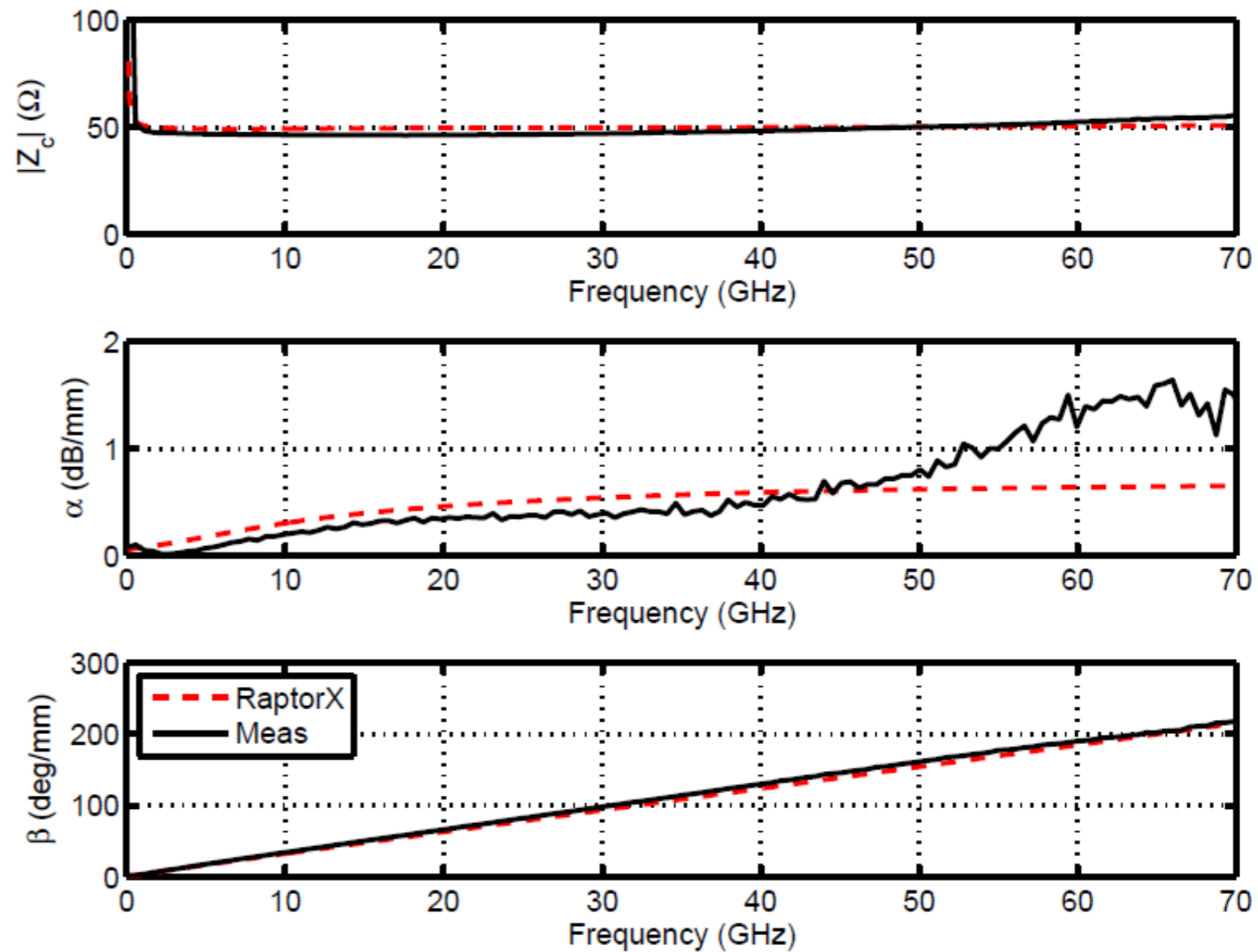
» SCPW T-line



$$Z_c = \sqrt{\frac{B}{C}}$$

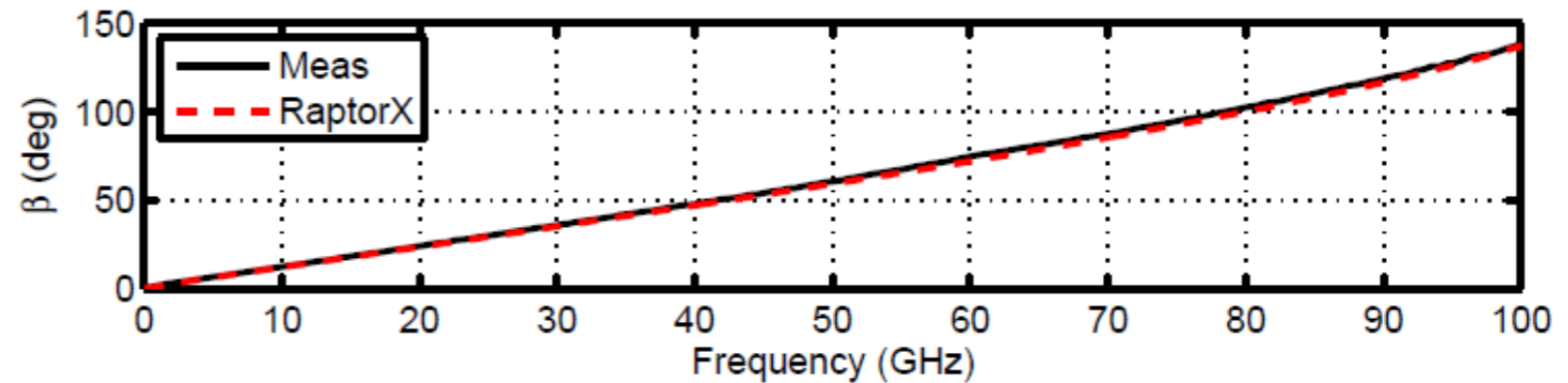
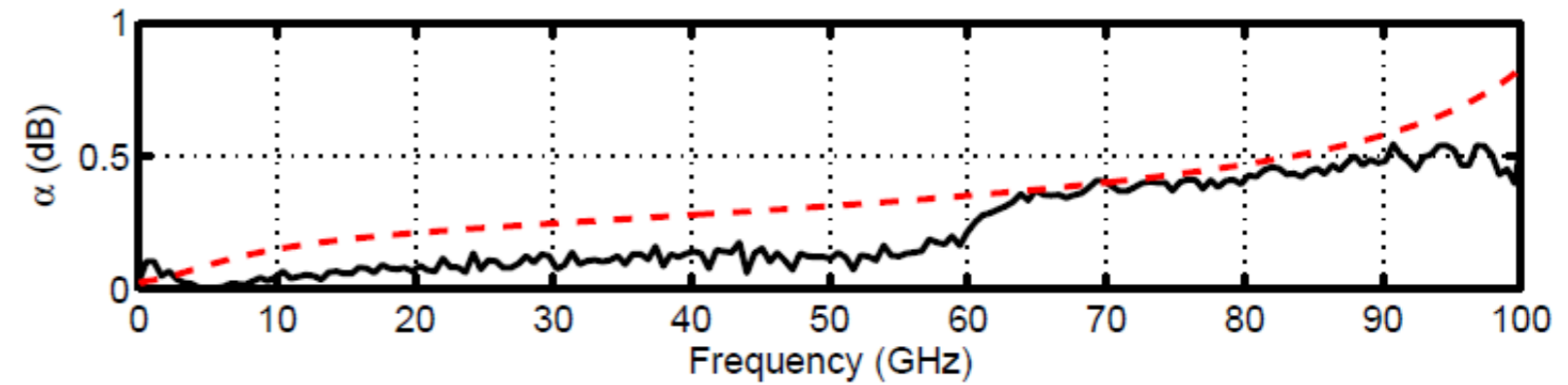
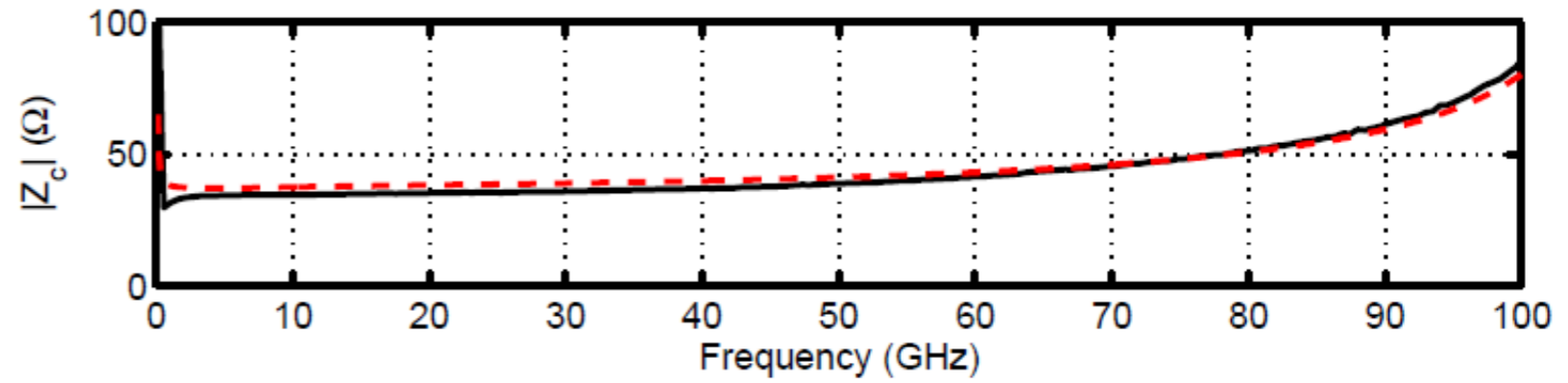
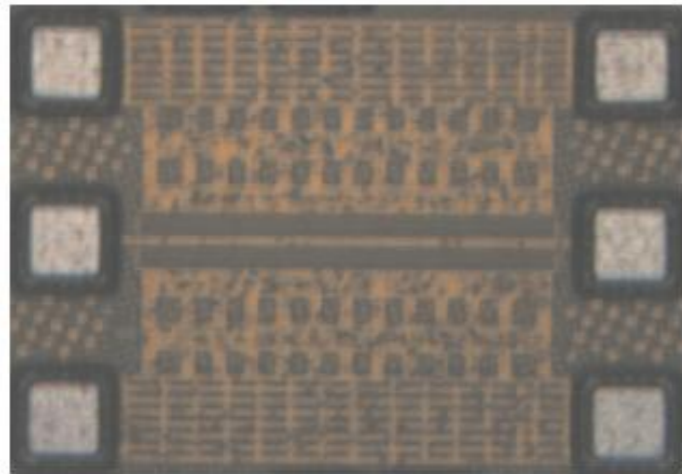
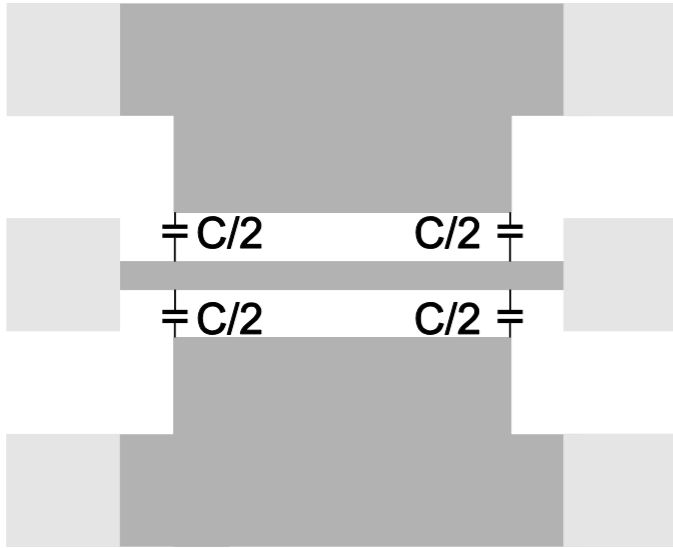
$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A))$$

$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A))$$



mm-wave Silicon – Semi-lumped

» CPW with MOMcap

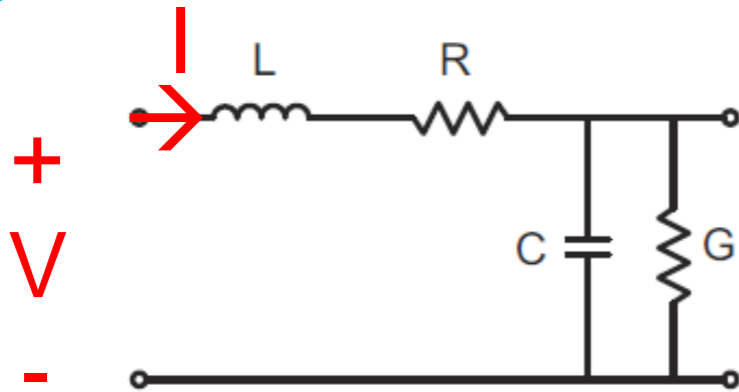




Model Everything

T-line Theory & Testbench

Theory



$$\frac{\partial V(x)}{\partial x} = -(R + j\omega L)I(x)$$

$$\frac{\partial I(x)}{\partial x} = -(G + j\omega C)V(x)$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Testbench



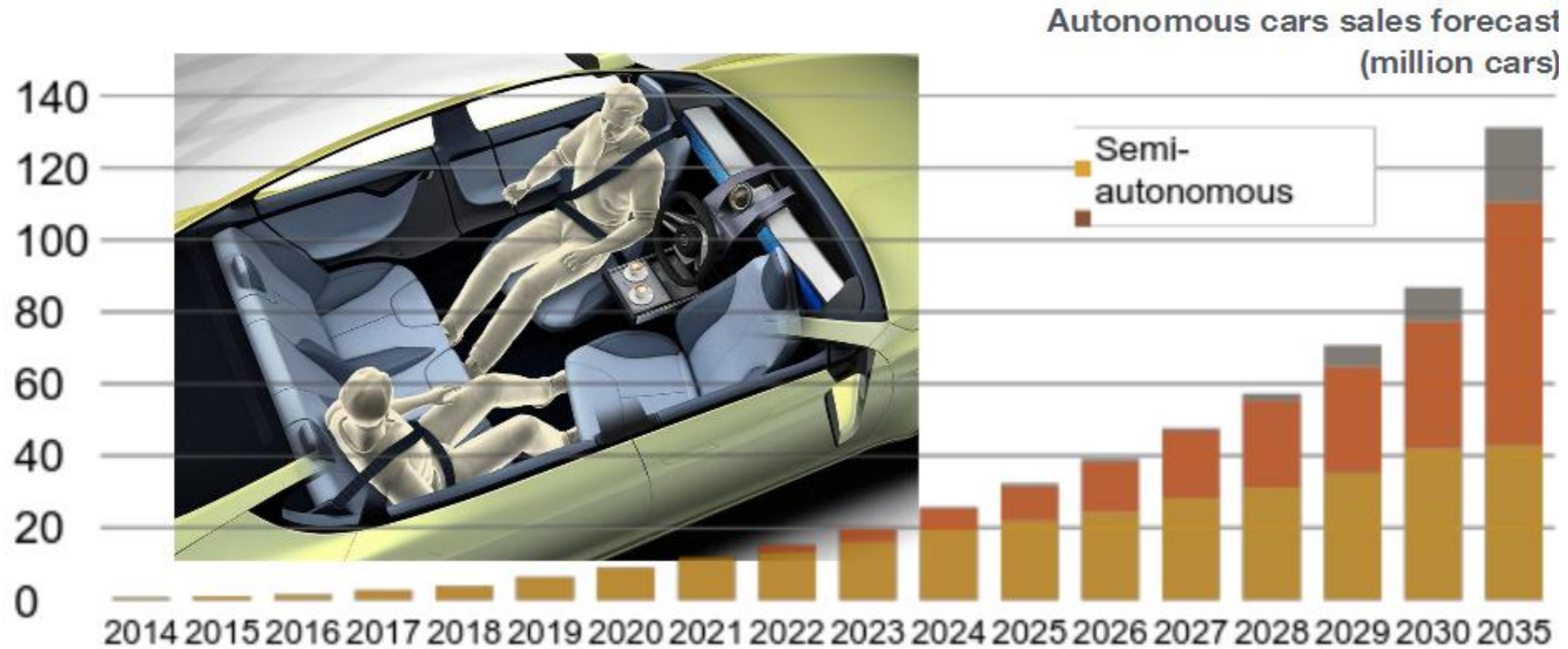
T-line metrics calculated from ABCD parameters

$$Z_c = \sqrt{\frac{B}{C}}$$

$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A))$$

$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A))$$

Driverless needs mm-wave nm CMOS



» Every car will be equipped with 10-20 radars to move on its own