Helic®

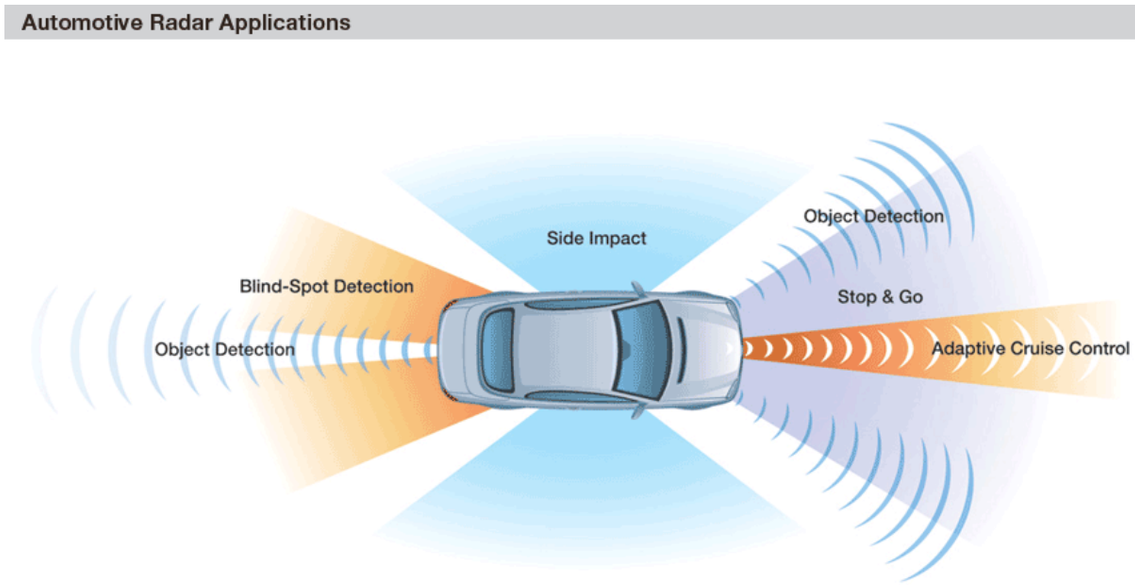
nm CMOS Device Synthesis for mm-Wave Design

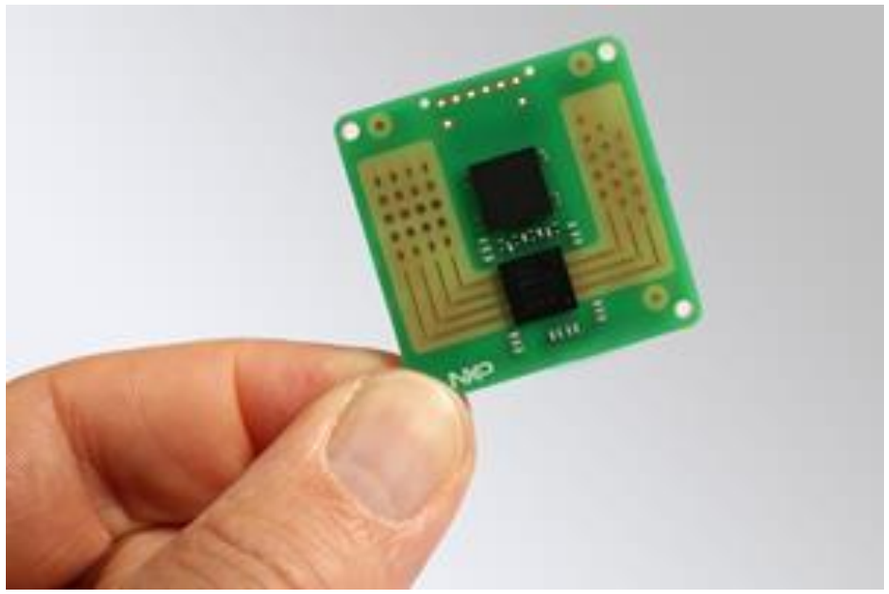
Errikos Lourandakis

CDNLive Munich, May 2-4 2016

Why mm-wave silicon design?

- nm CMOS mm-wave device synthesis
  - Automotive radar 77-81GHz





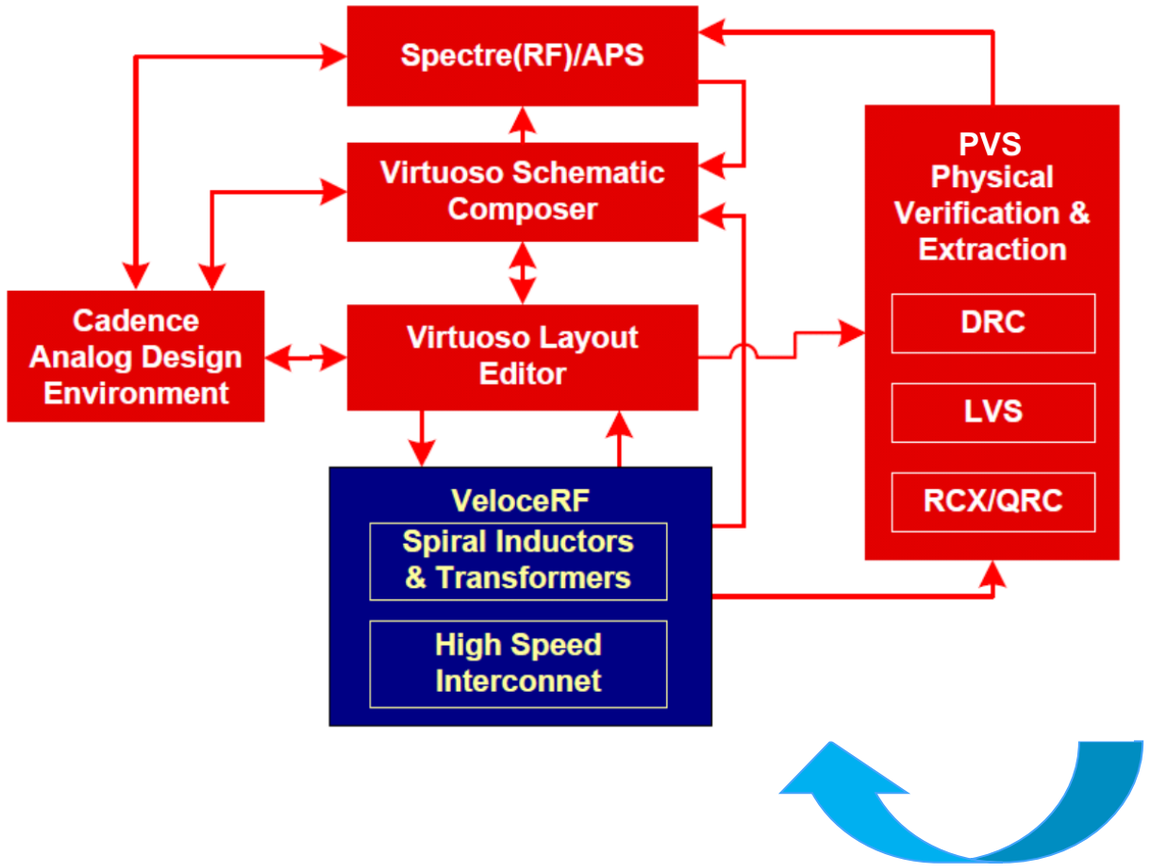
Source: NXP, CES 2016

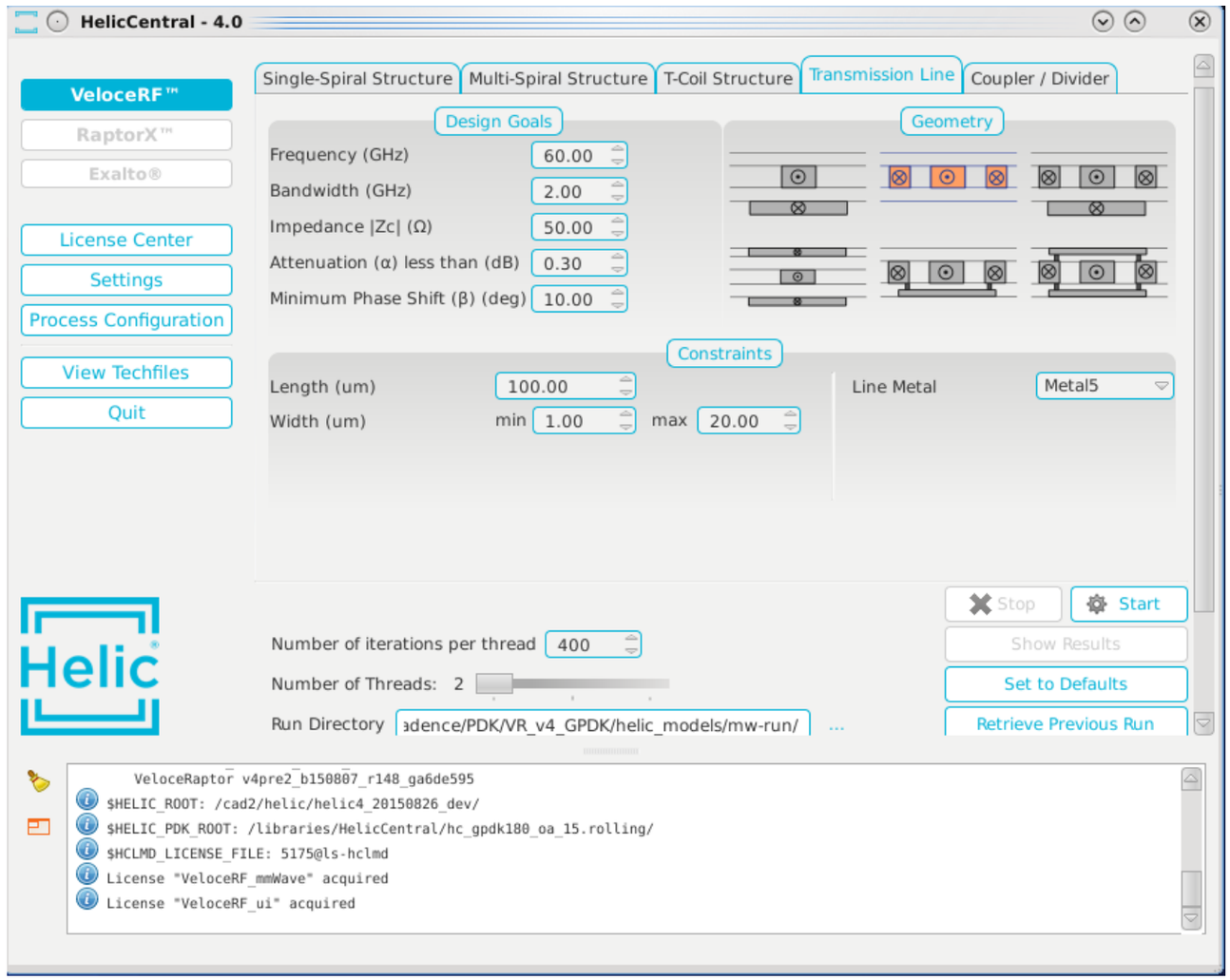
- Long range and short range radar around vehicle for advanced driver assistance systems (ADAS)
- Existing solutions in SiGe and now CMOS
- Demand for ADAS is massive ~ Millions of units/year

mm-wave silicon with Helic

- Helic's PCell synthesis inside Cadence Virtuoso
  - mm-wave Transmission Lines, Bends, Junctions
  - mm-wave Couplers
  - DRC, LVS clean SKILL PCells
  - Schematic and layout views for Cadence PVS flow
  - RLCk and S-par models suitable for frequency and time domain analyses within Virtuoso ADE
- PCell synthesis down to 7nm/10nm/16nm CMOS

Where does Helic come into play?

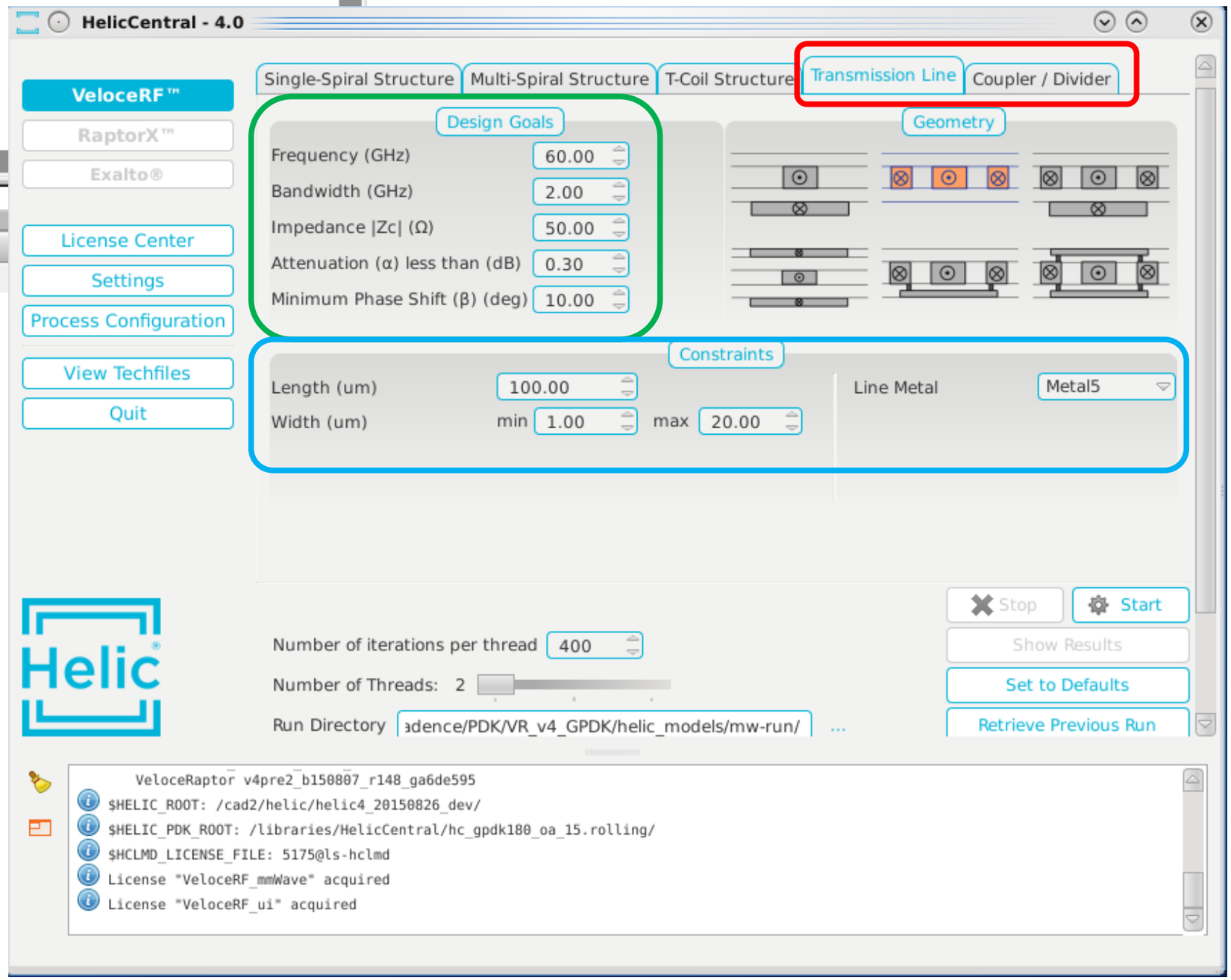




- mm-wave device synthesis integrated in Cadence
- Transmission lines, bends and couplers
- DRC, LVS clean PCells ready for mm-wave design

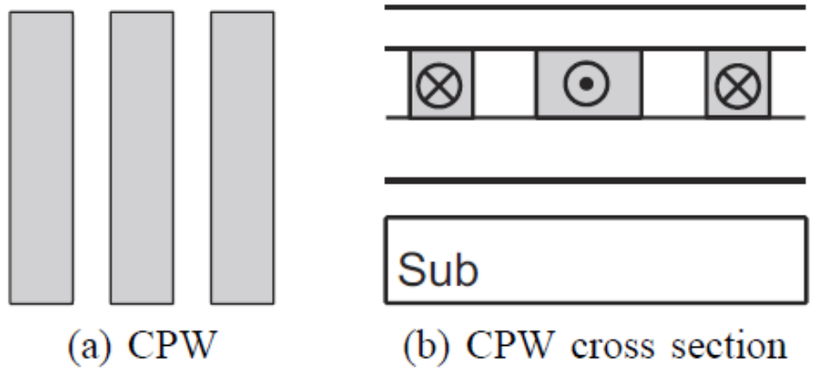
mm-wave Device Synthesis

mm-wave PCells

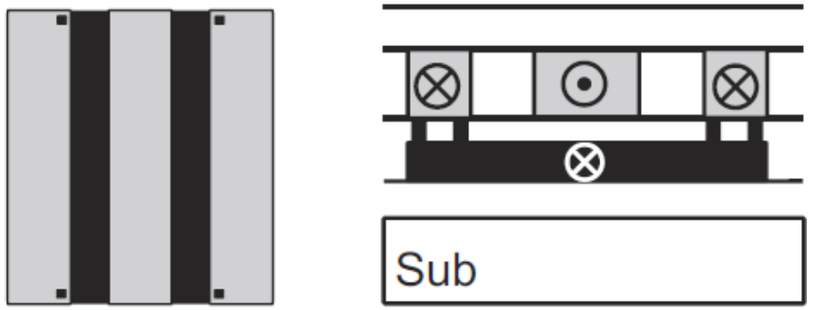


- HelicCentral Suite seamlessly integrated in Cadence Virtuoso
- VeloceRF mm-wave
- User defined constraint driven mm-wave device synthesis

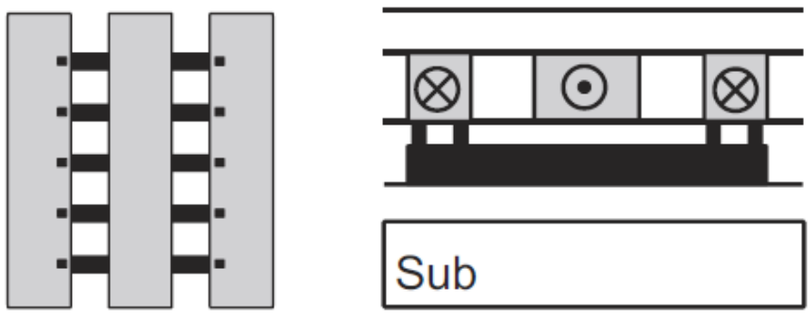
CMOS Transmission Lines



(a) CPW (b) CPW cross section

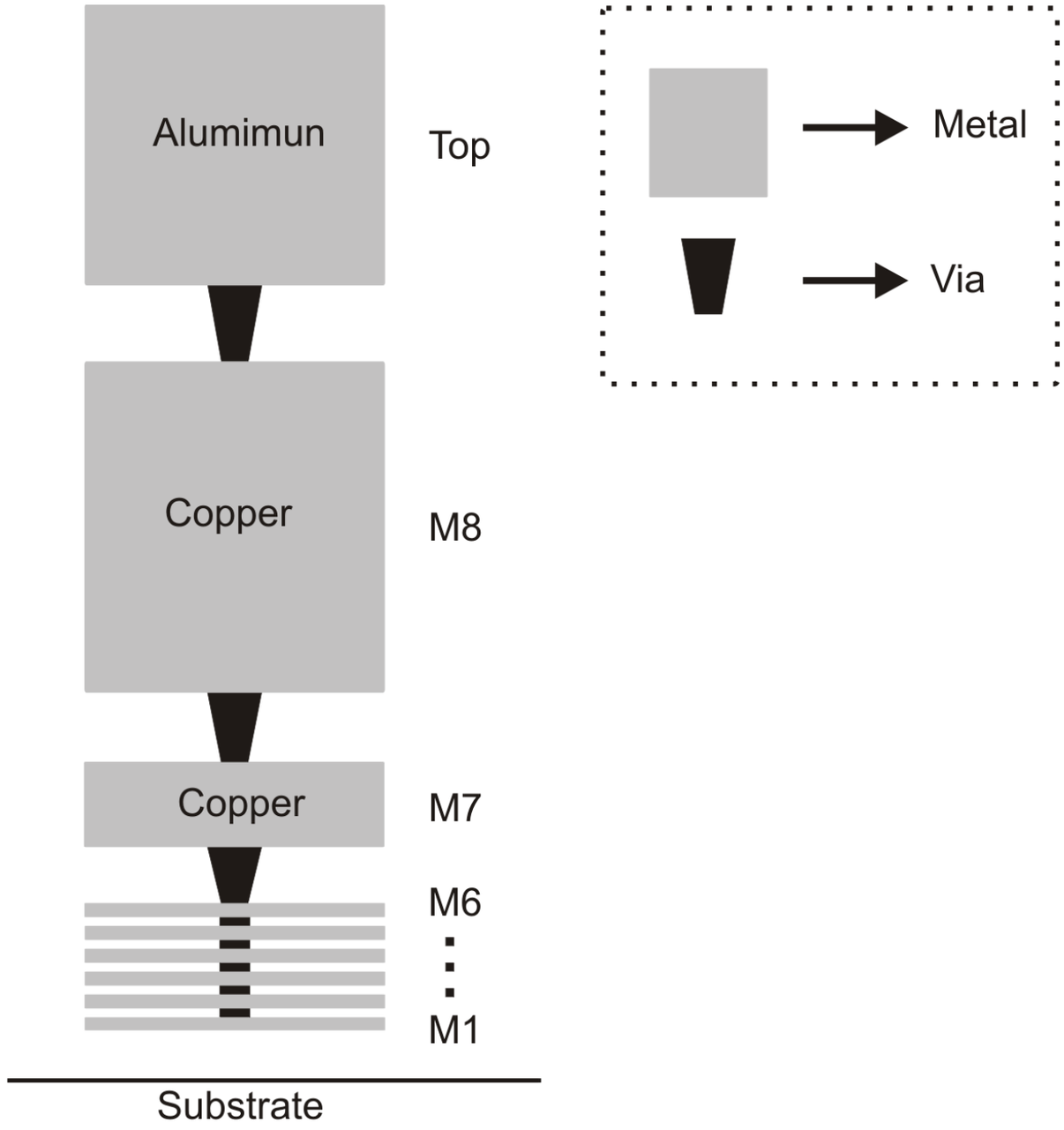


(c) CPWG (d) CPWG cross section

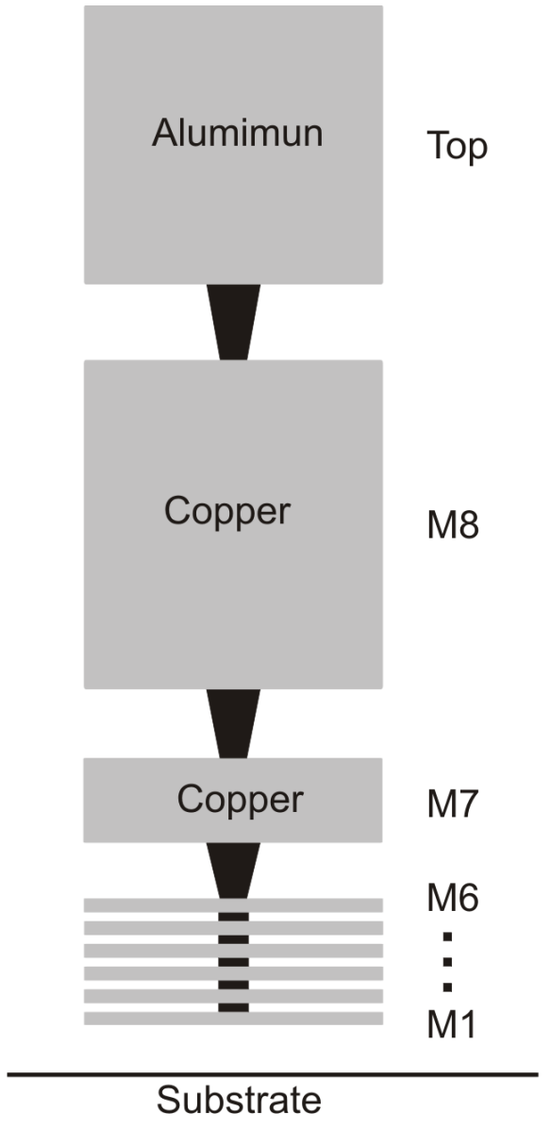


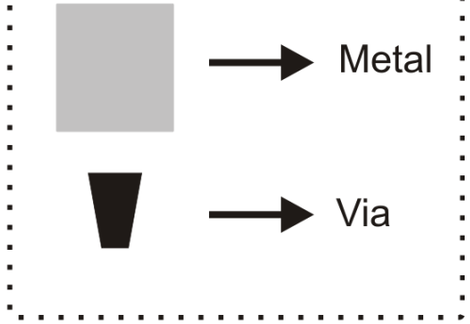
(e) SCPW (f) SCPW cross section

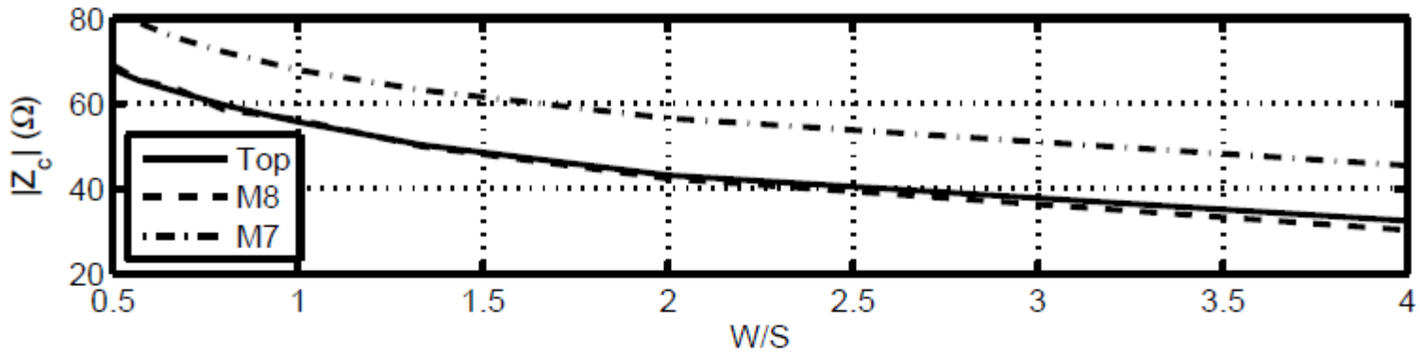
Simplified 40nm CMOS BEOL

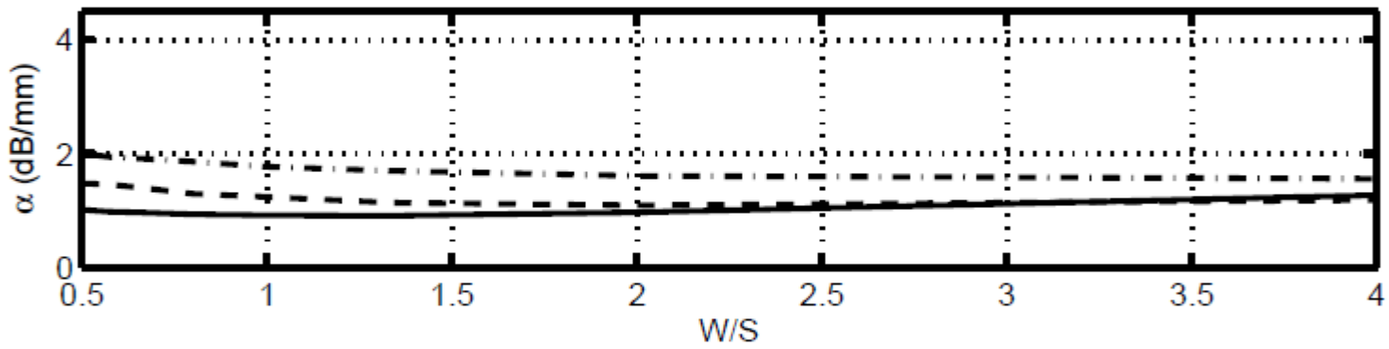


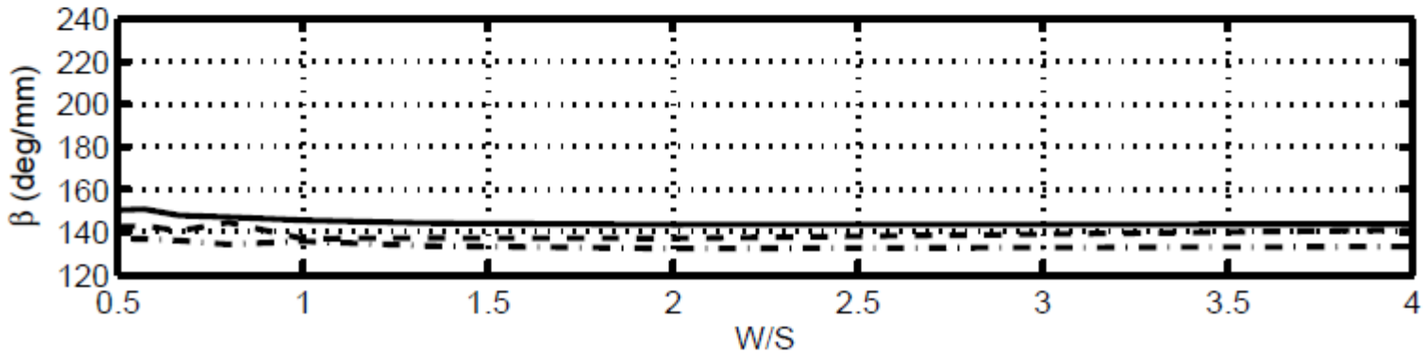
Where is the challenge?





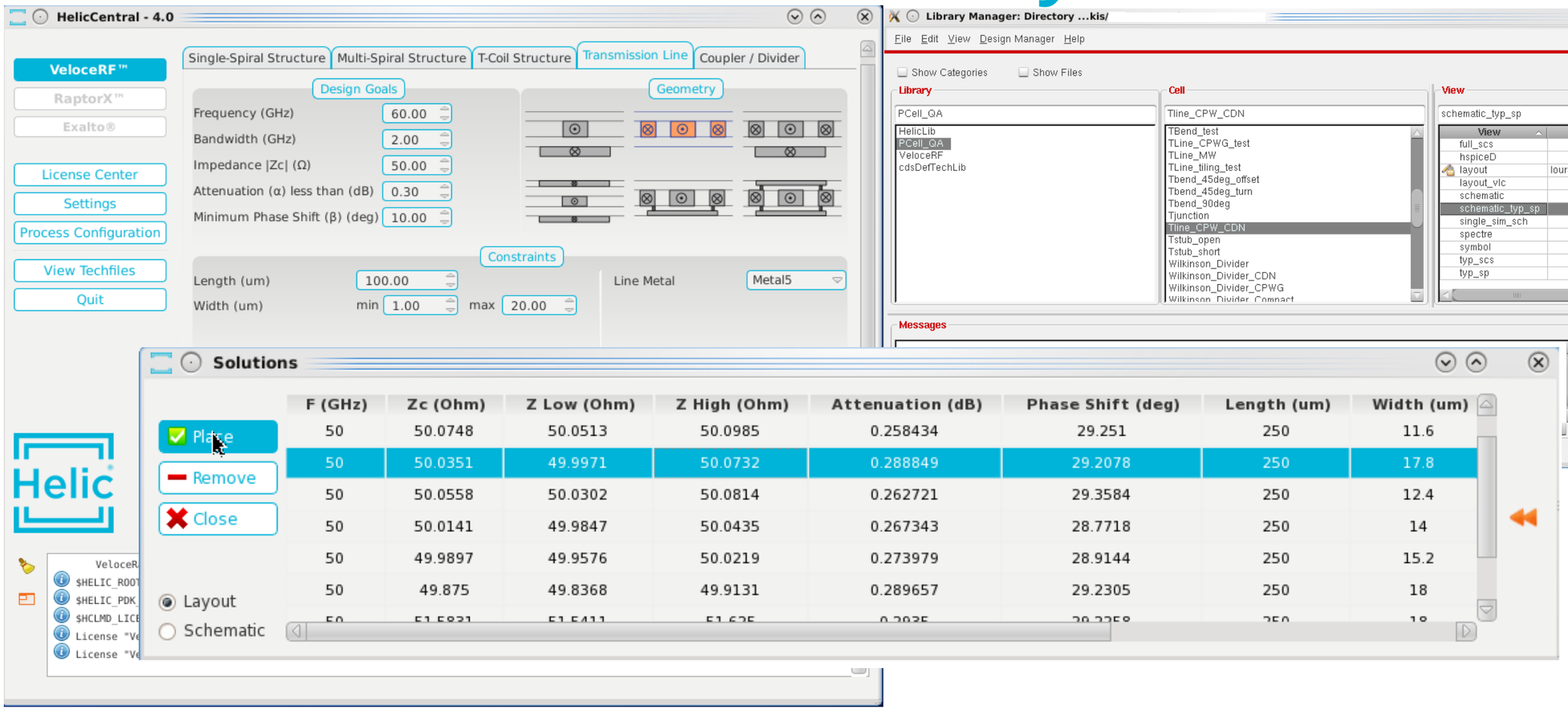






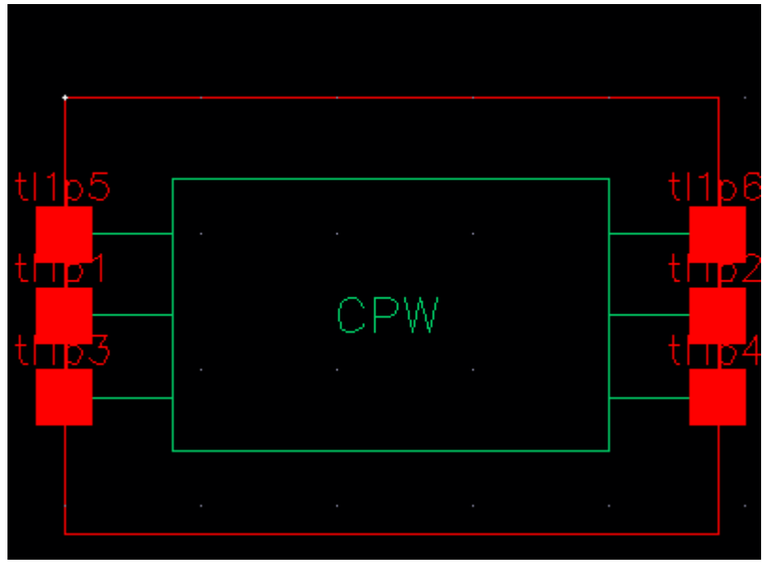
- CPW T-line example
- Parametric analysis @ 60GHz

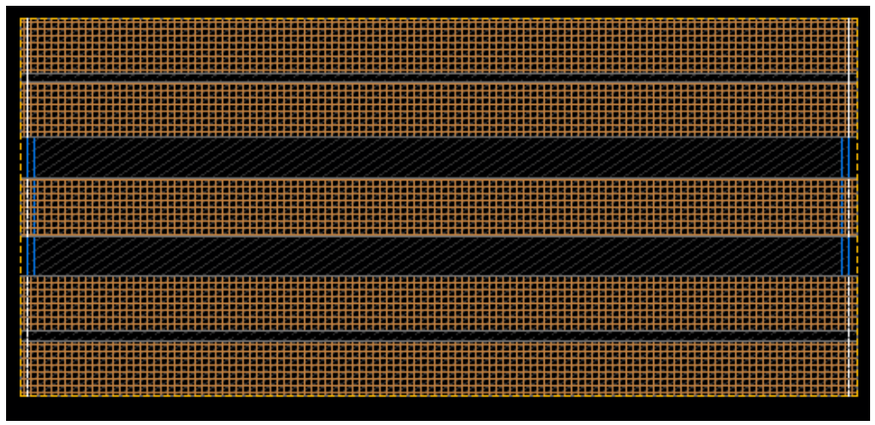
mm-wave T-line Synthesis

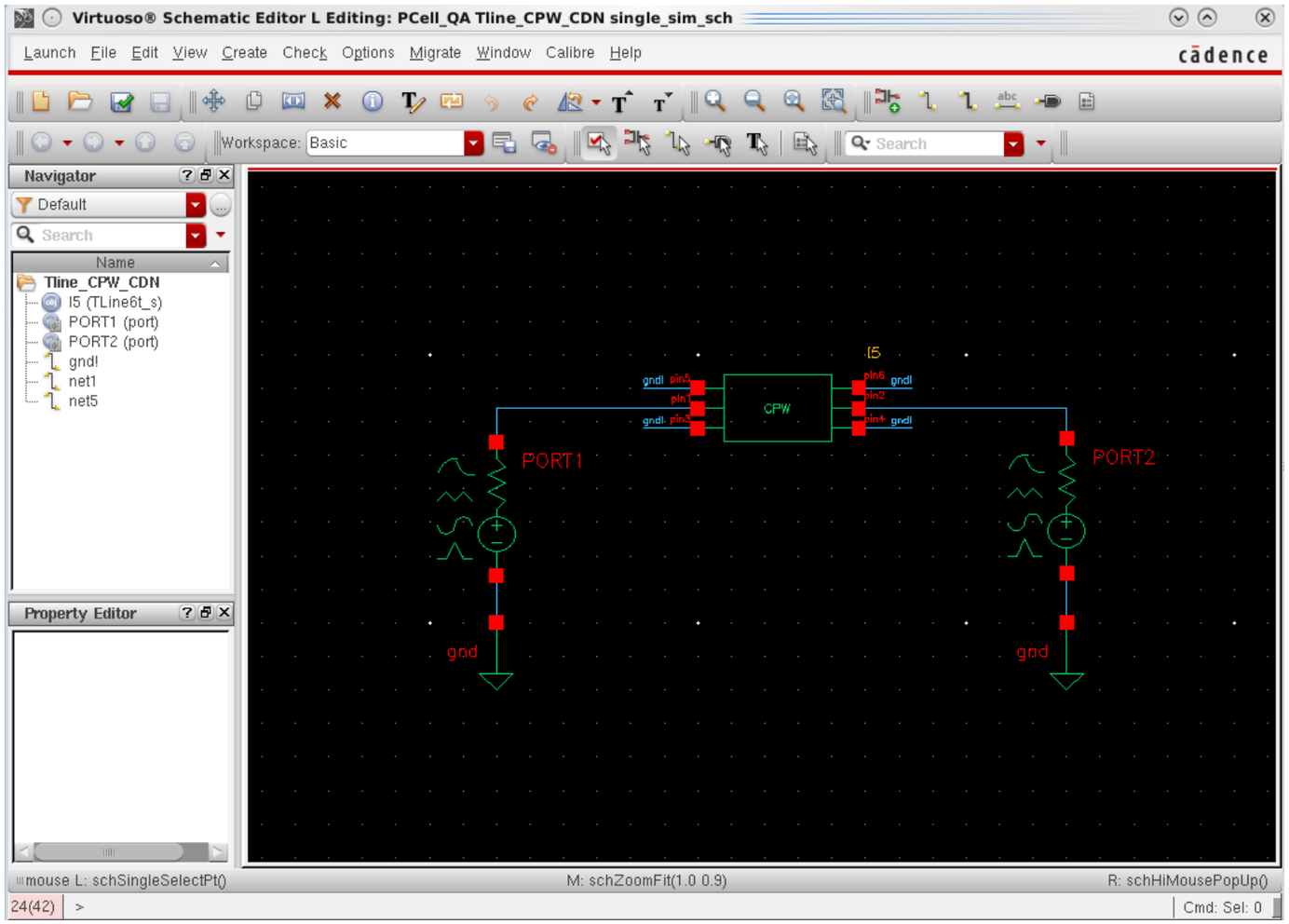


- Synthesis returns multiple solutions matching user defined constraints
- Layout, schematic, and symbol views including RLCk model at your finger tips

Registered DFII views

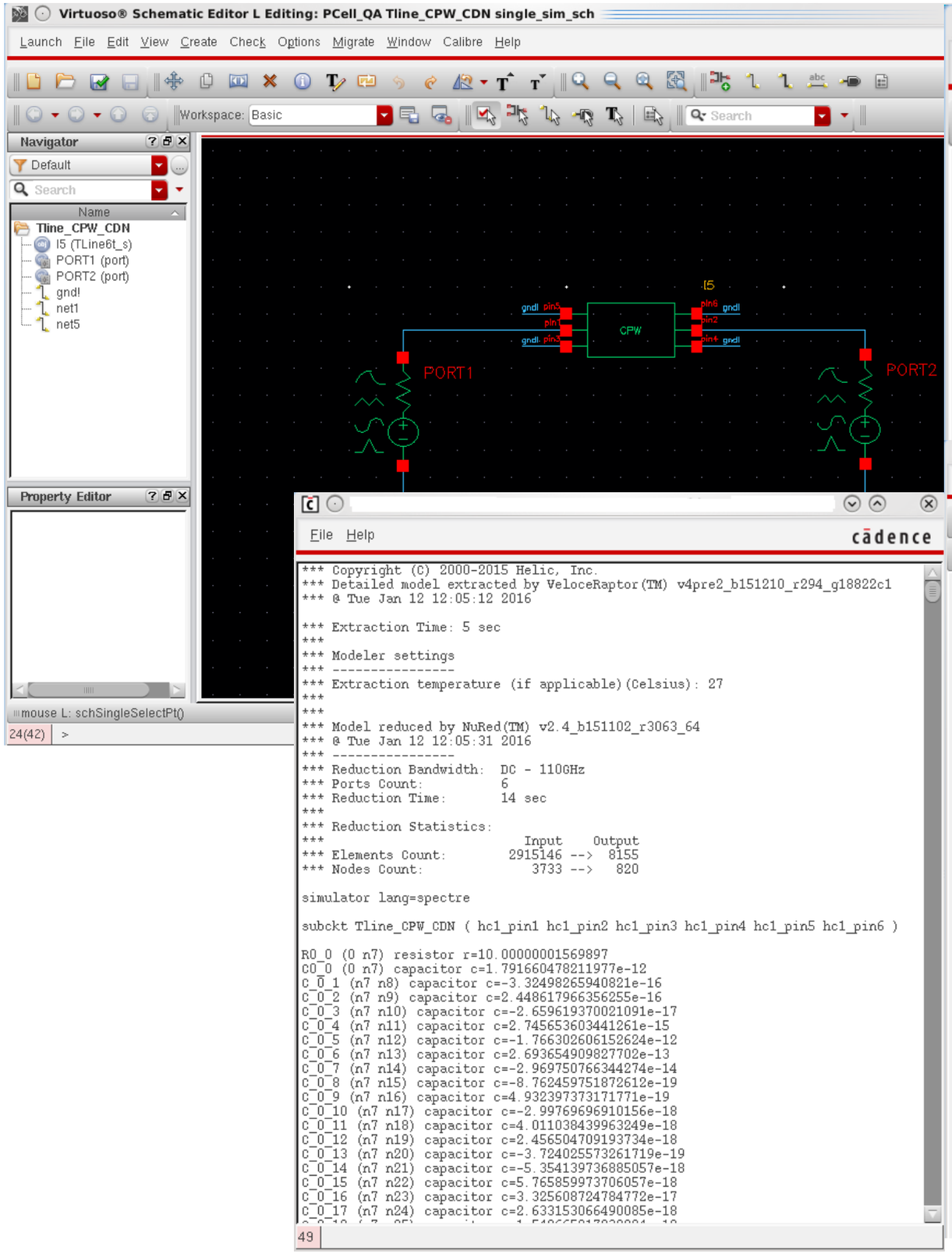




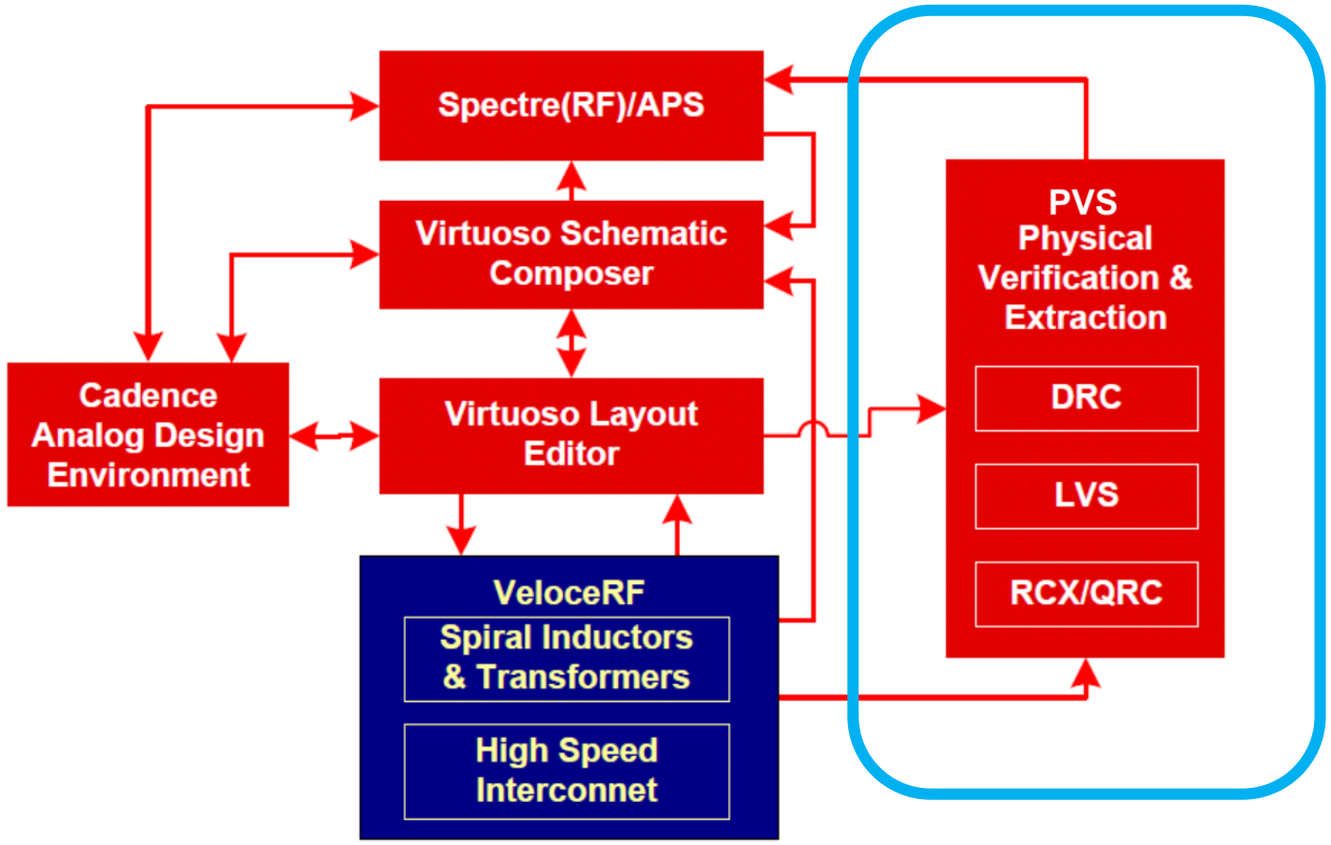


- Automatically generated testbench
- Device model suitable for frequency and time domain analyses in ADE

PCell verification using Spectre

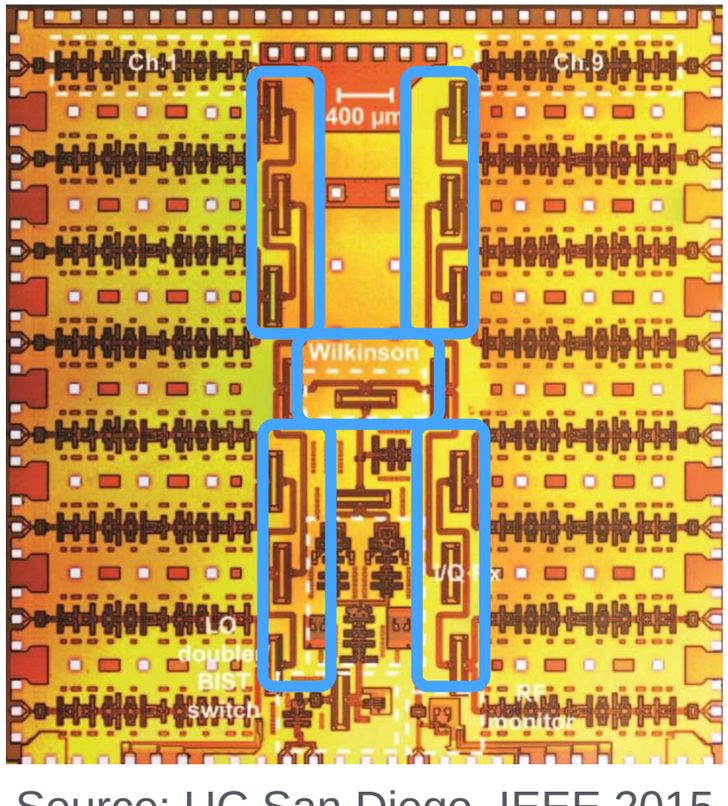


Integration to Physical Verification

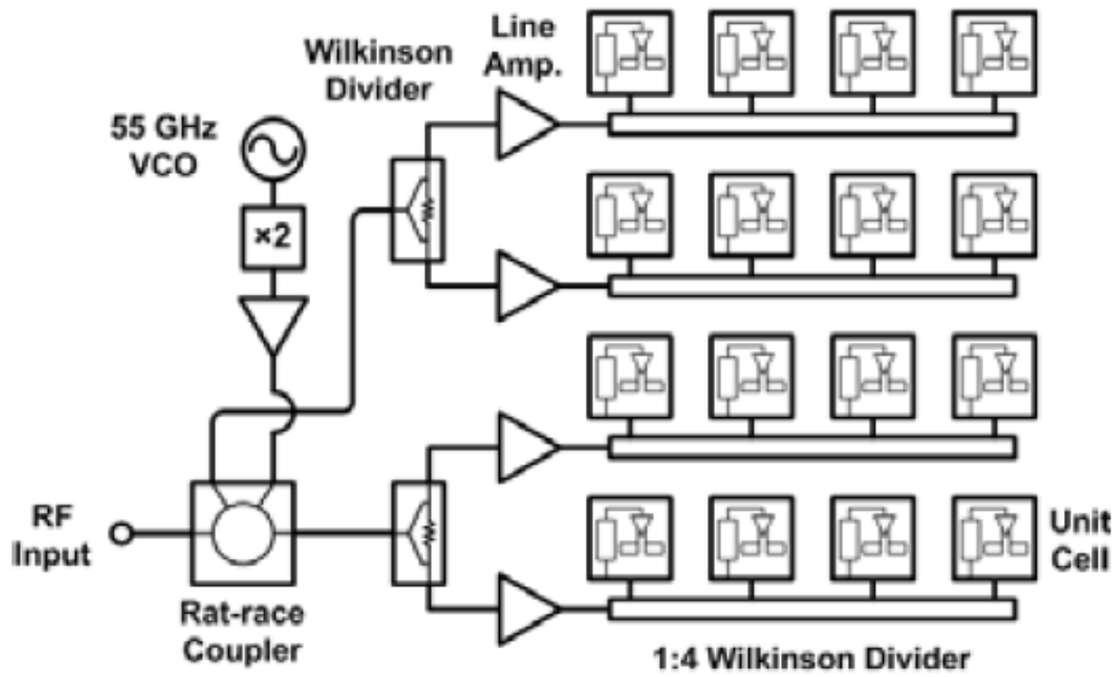


- PCell inserted in top-level layout
- User runs PVS DRC, LVS as usual in top-level layout
- Quantus QRC invoked from layout for extracting parasitic components of entire circuit

Are mm-wave passives relevant?



Source: UC San Diego, IEEE 2015
Multi-channel 77-81GHz SiGe radar



Source: UC San Diego, IEEE 2015
110 GHz Transmit Phased Array Topology

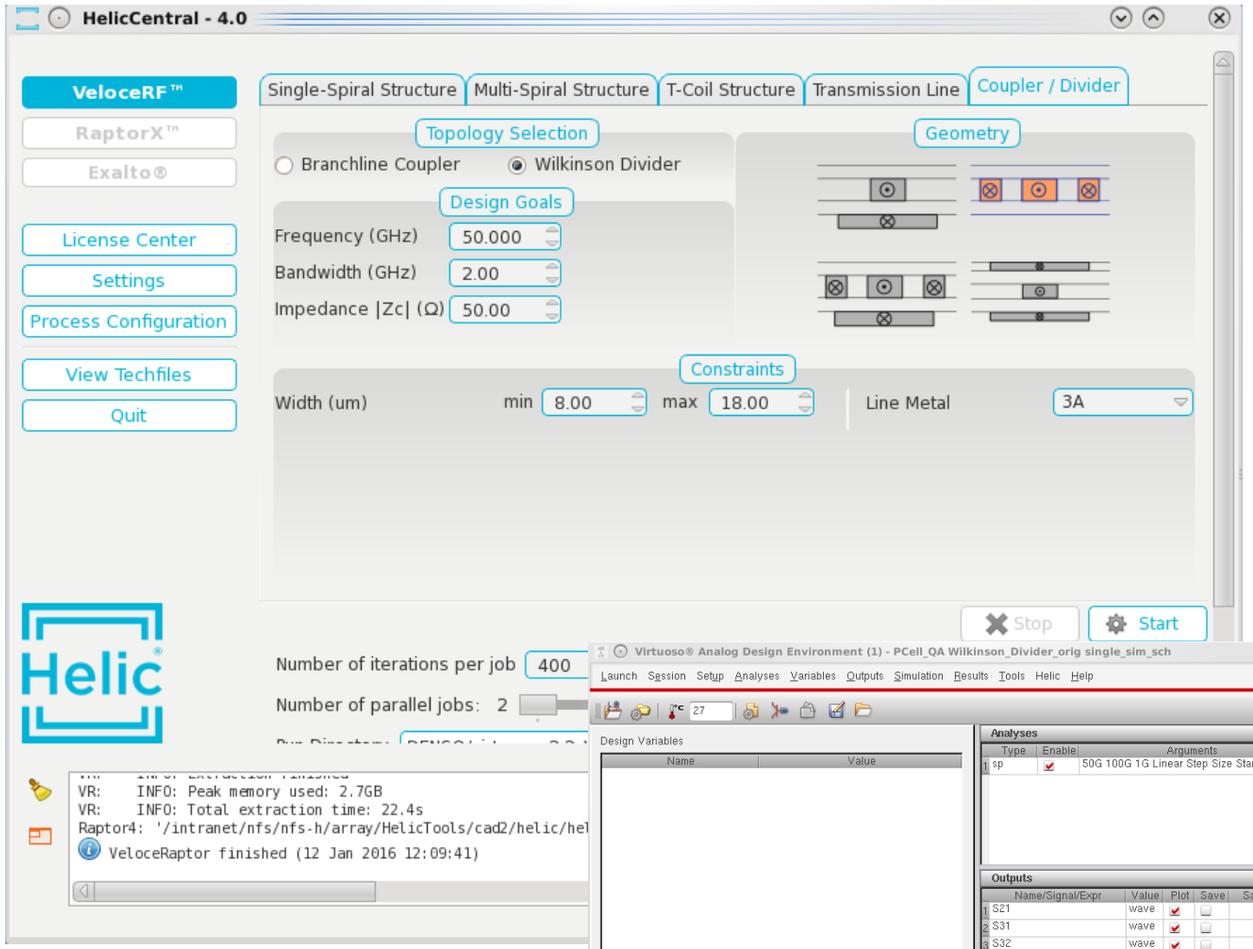
- T-lines and mm-wave couplers (e.g. Wilkinson divider) are key building blocks
- Physics for nm CMOS design are complex
- Automated and constraint driven design is needed

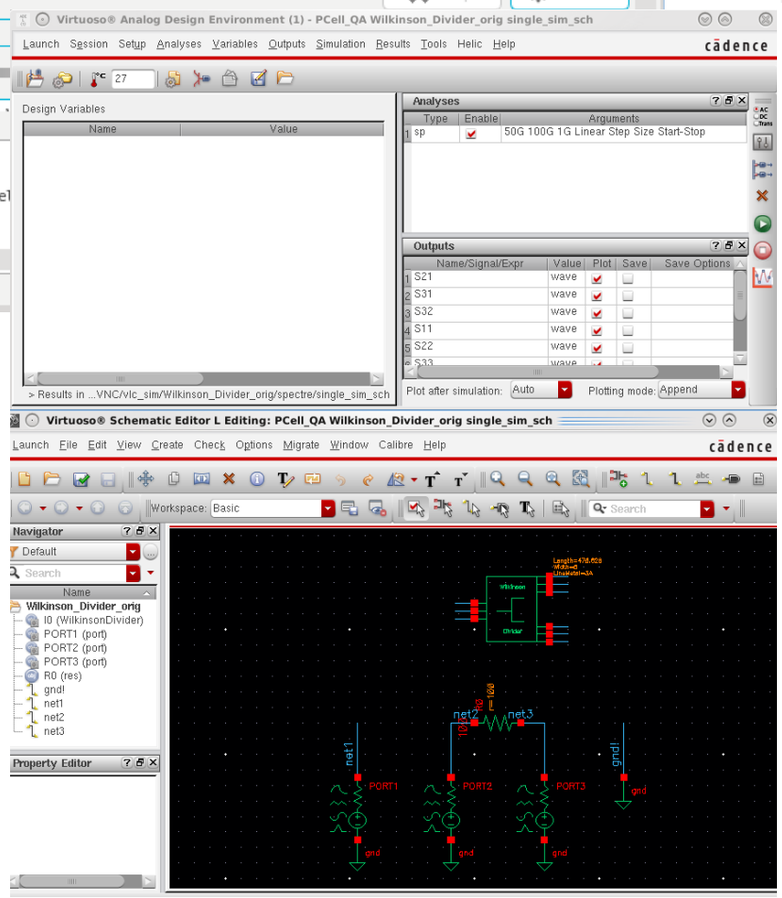
Helic’s unique mm-wave flow

- Example 1
  - Synthesis of Wilkinson divider by VeloceRF
  - 77-81GHz tuned divider
  - Fully customizable PCell in Cadence (DRC, LVS, PVS compliant)

- Example 2
  - Custom Wilkinson divider design based on Helic’s mm-wave PCells (T-lines, Bends and Junctions)
  - 77-81GHz tuned divider
  - Custom device for Cadence verification flow

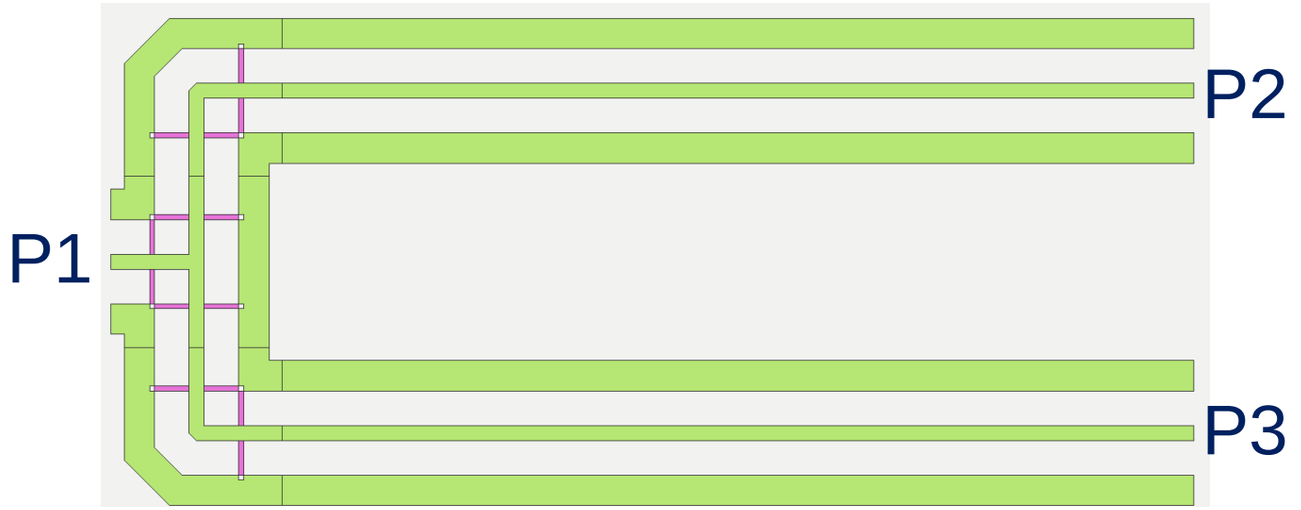
Example 1 – Divider PCell

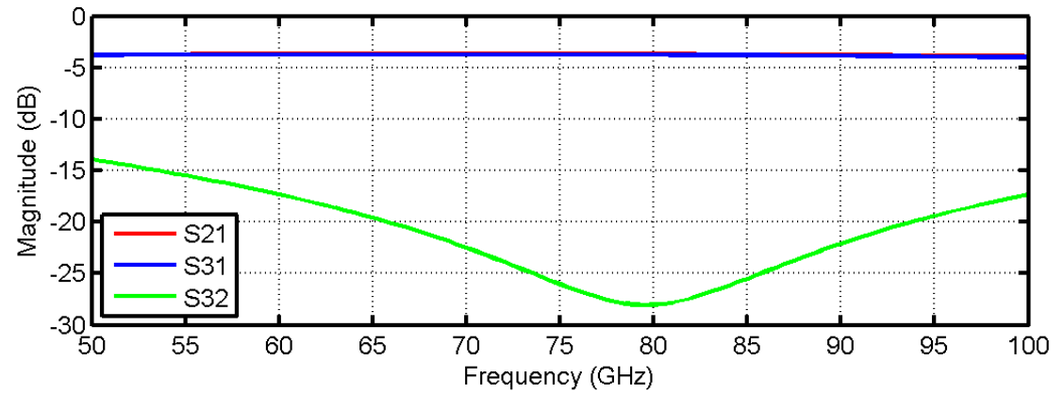


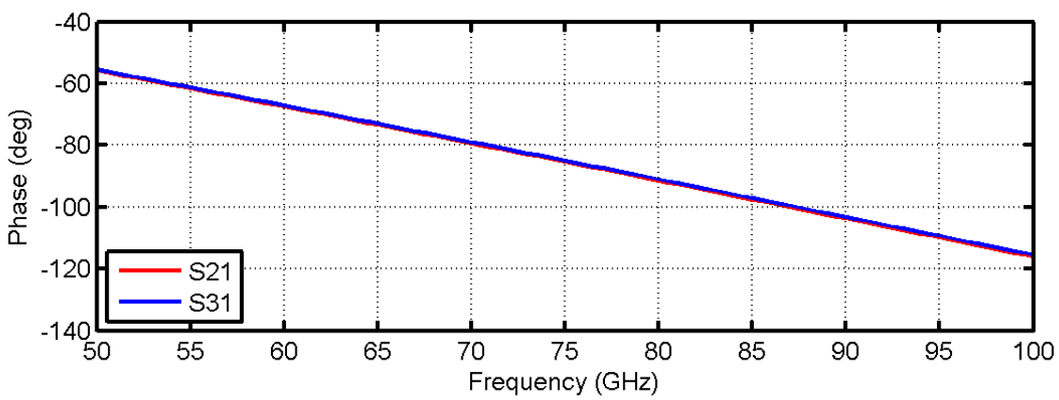


- Automated and faster synthesis
- Schematic / Layout view
- Simulate device in ADE

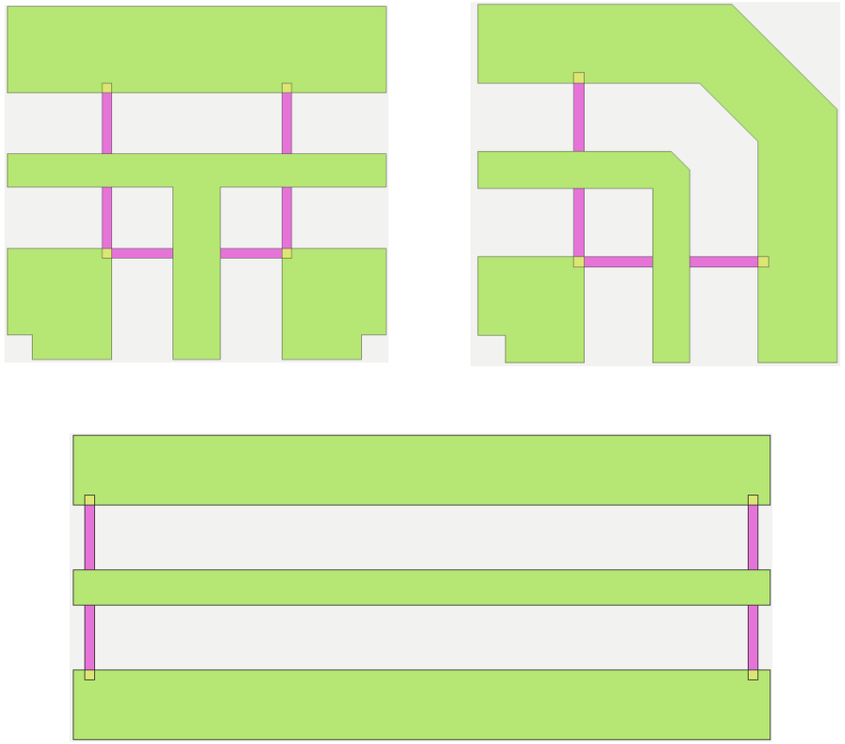
Area: 0.0871mm²



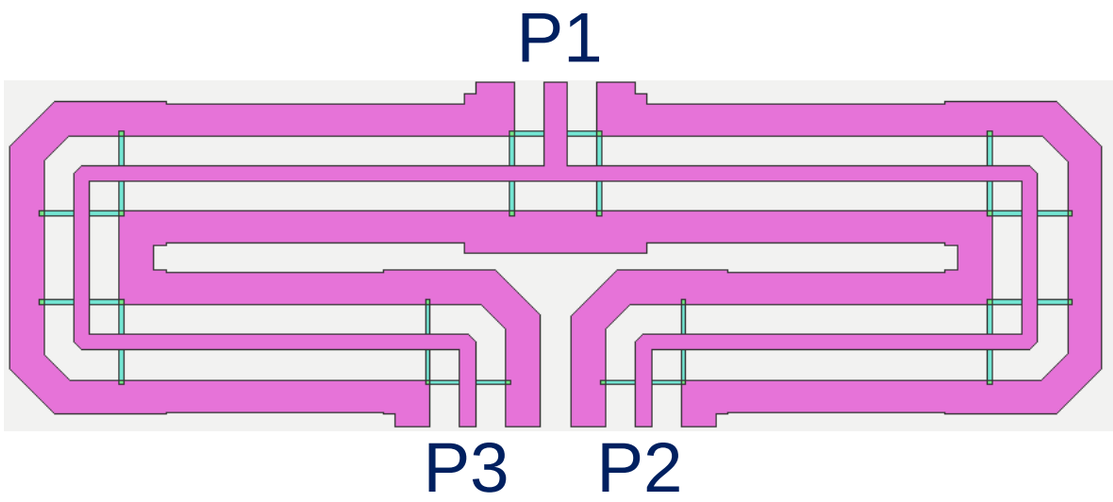


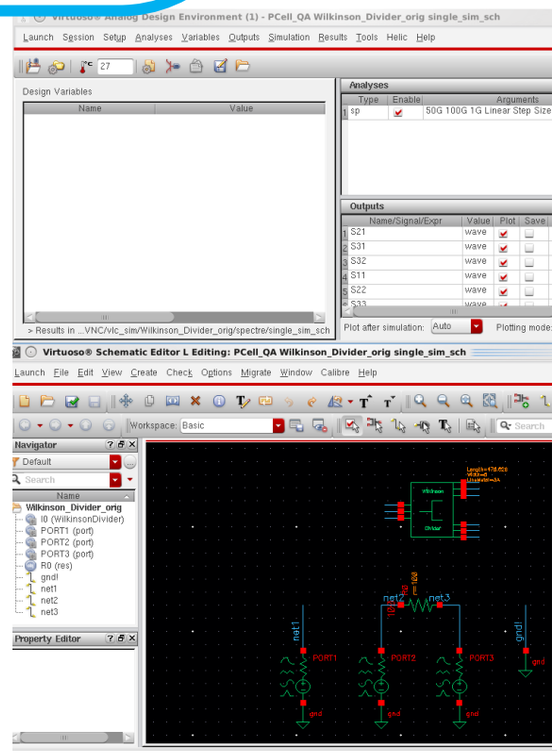


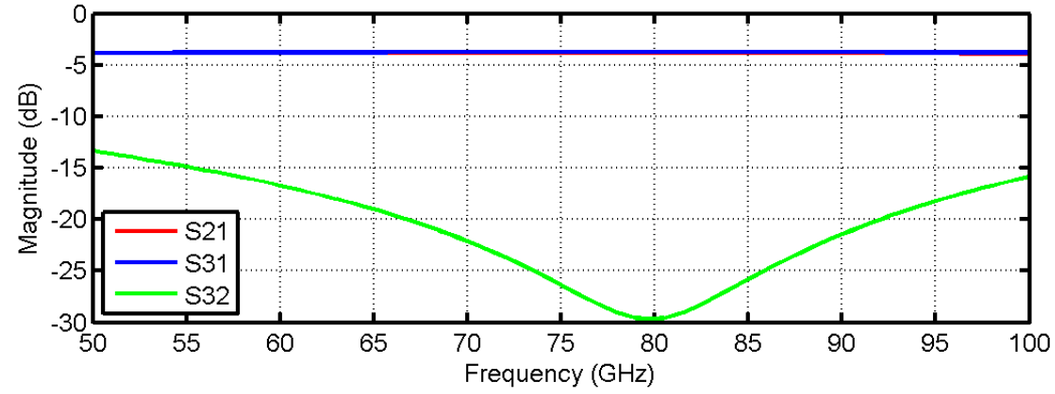
Example 2 – Custom Design

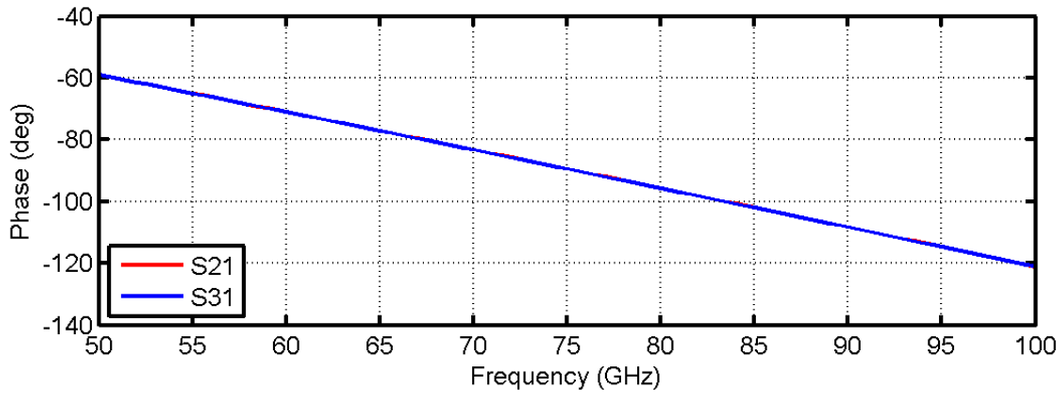


Area: 0.0744mm^2



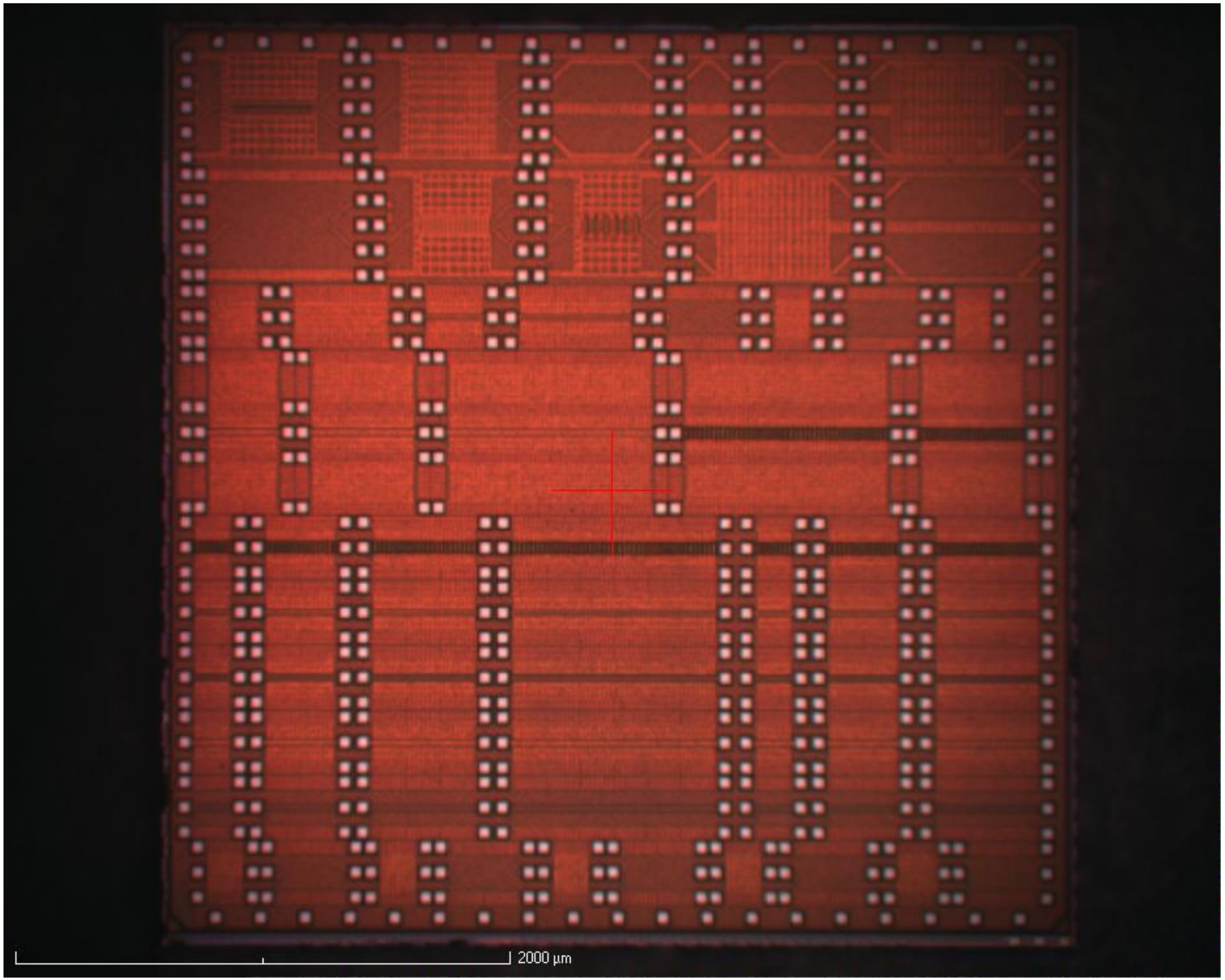






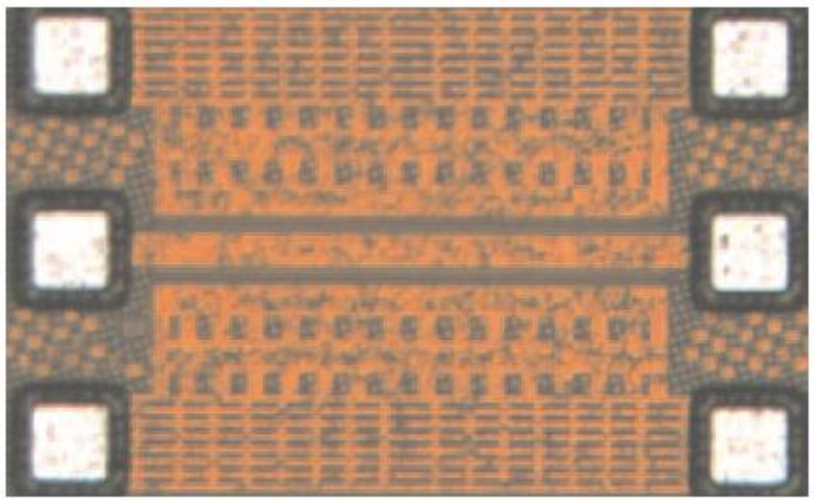
- PCells used for area optimized design
- Smaller footprint
- Custom Device

mm-wave 40nm CMOS test chip

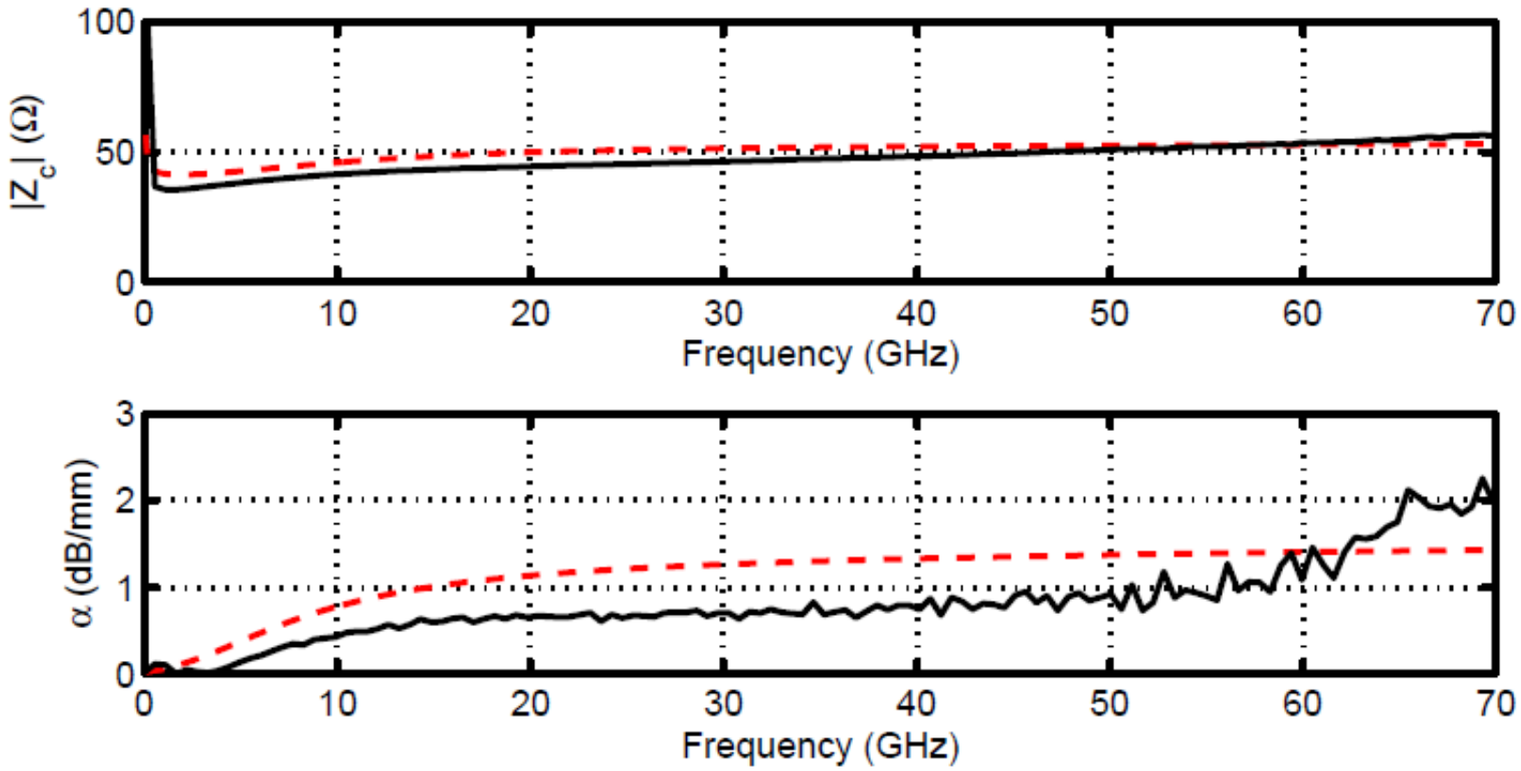


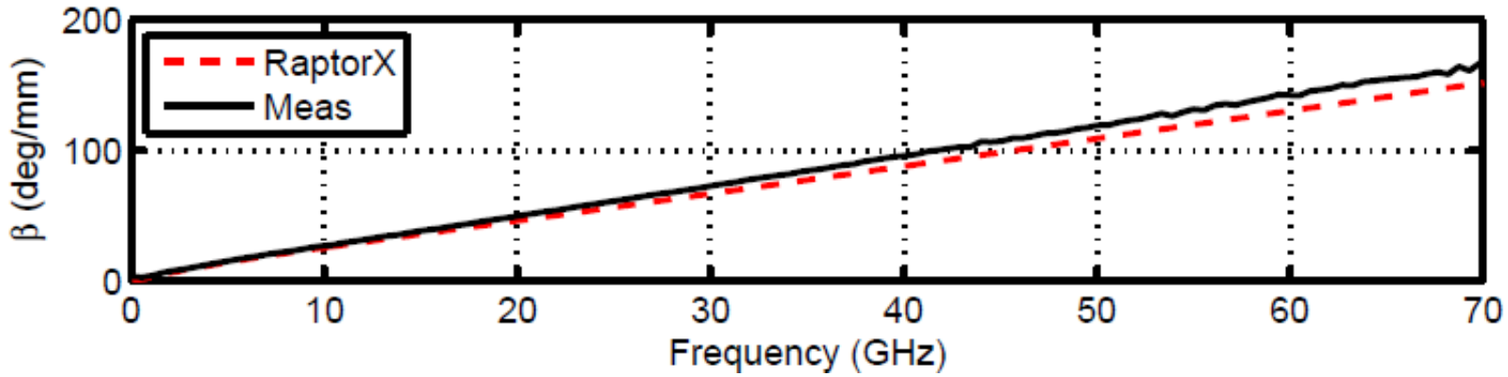
mm-wave Silicon – CPW

- CPW T-line



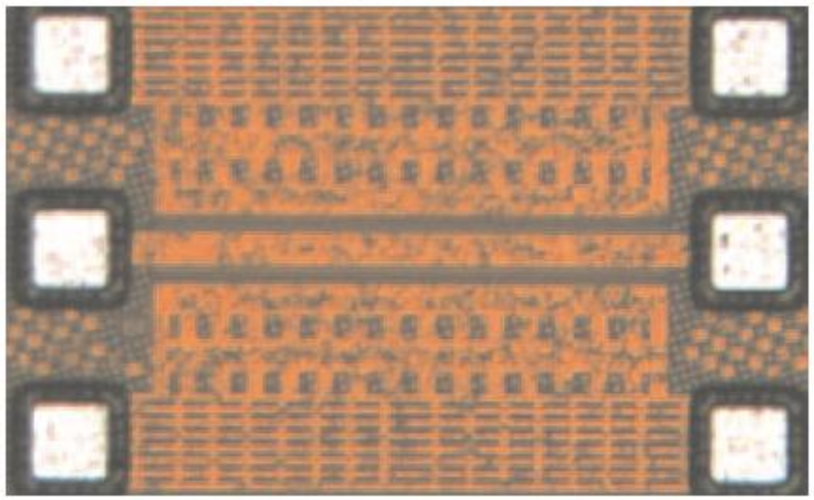
$$
\begin{aligned}
Z_c &= \sqrt{\frac{B}{C}} \\
\alpha &= 8.6859 \cdot \Re(cosh^{-1}(A)) \\
\beta &= (180/\pi) \cdot \Im(cosh^{-1}(A))
\end{aligned}
$$



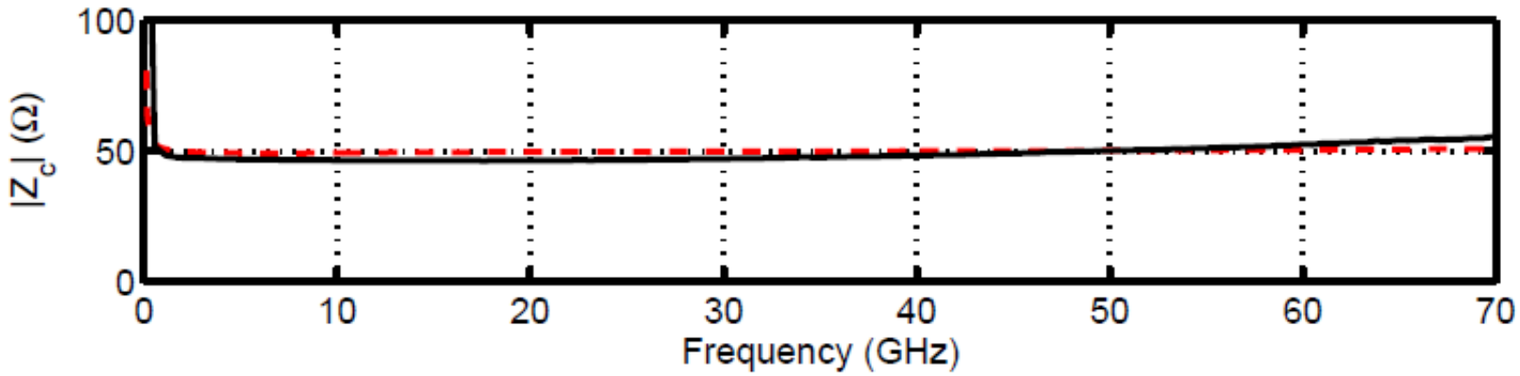


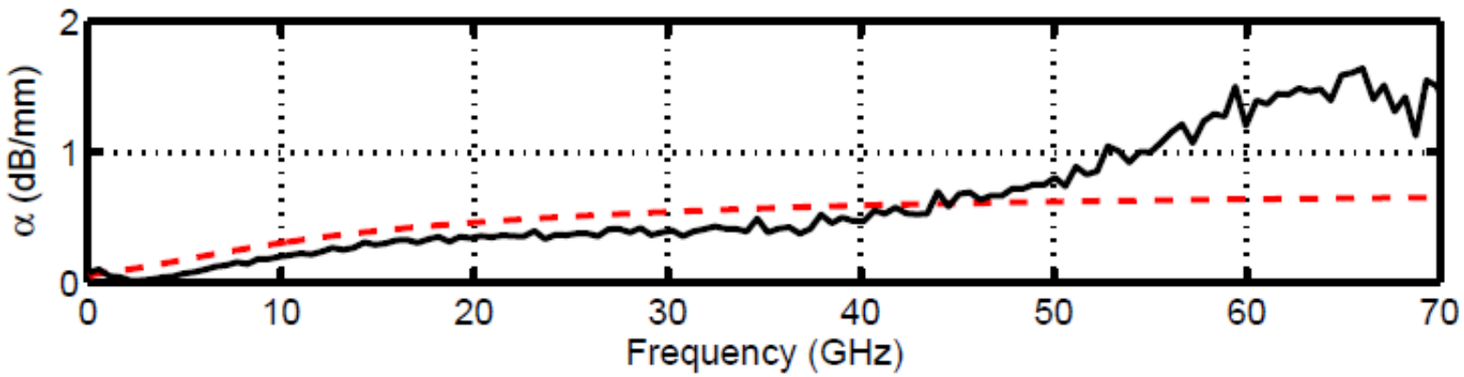
mm-wave Silicon – SCPW

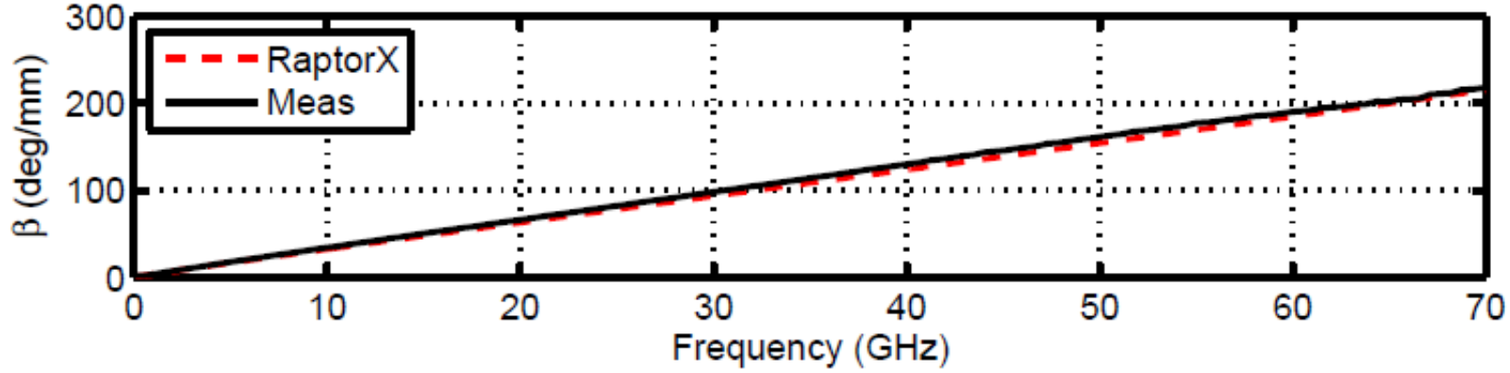
- SCPW T-line



$$
\begin{aligned}
Z_c &= \sqrt{\frac{B}{C}} \\
\alpha &= 8.6859 \cdot \Re(cosh^{-1}(A)) \\
\beta &= (180/\pi) \cdot \Im(cosh^{-1}(A))
\end{aligned}
$$

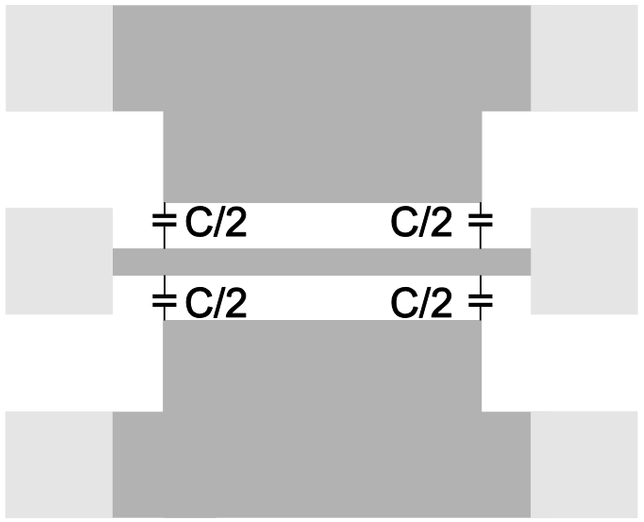


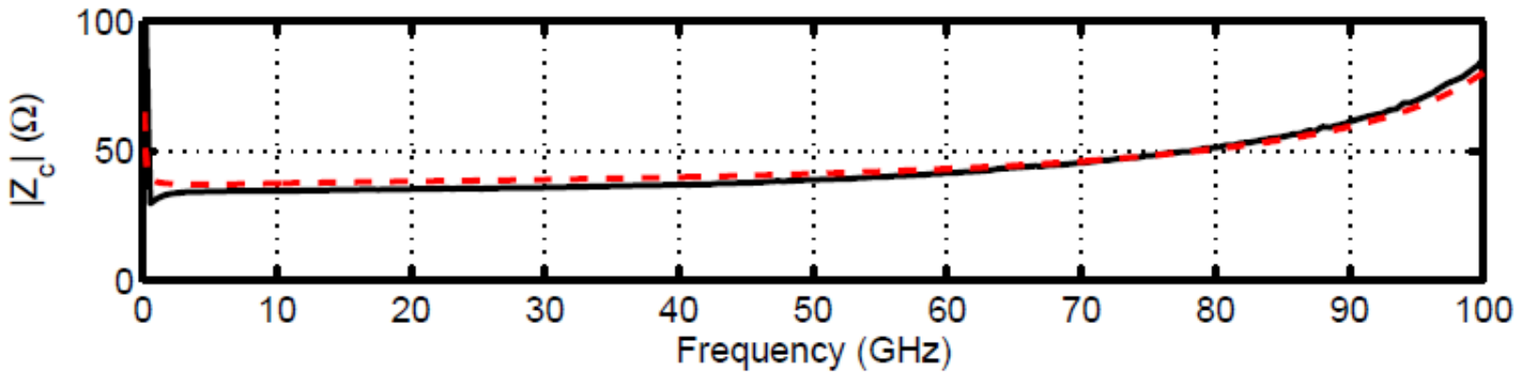


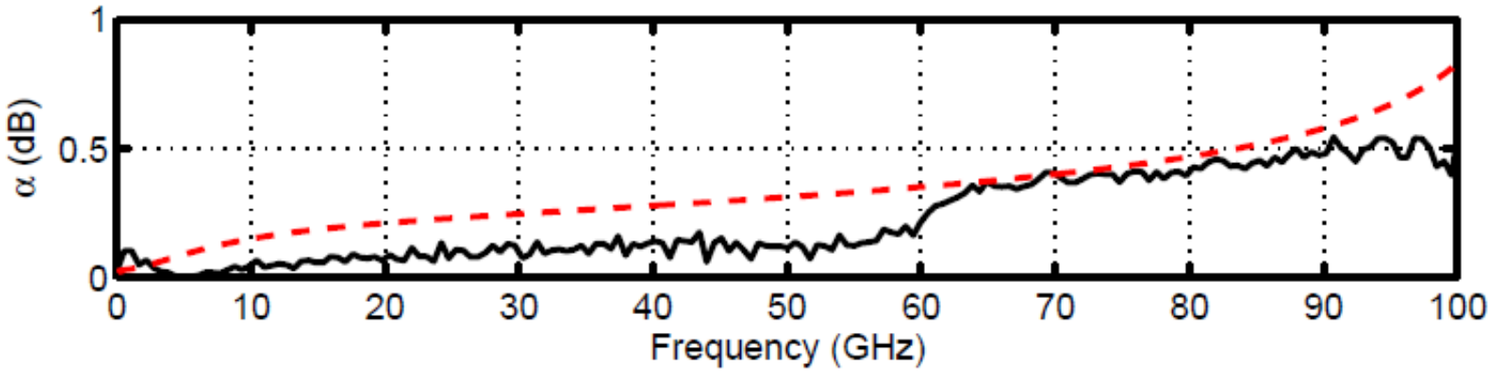


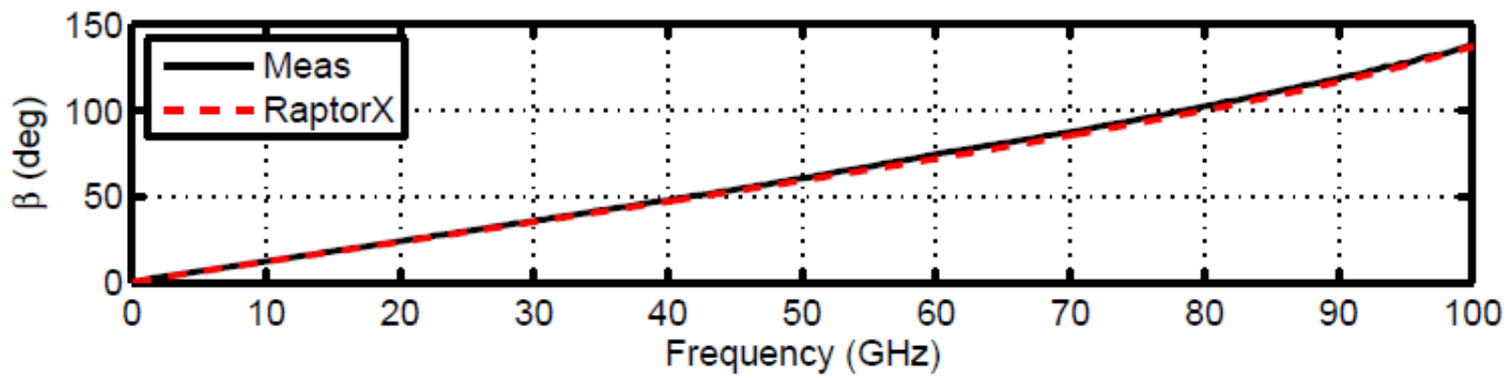
mm-wave Silicon – Semi-lumped

- CPW with MOMcap





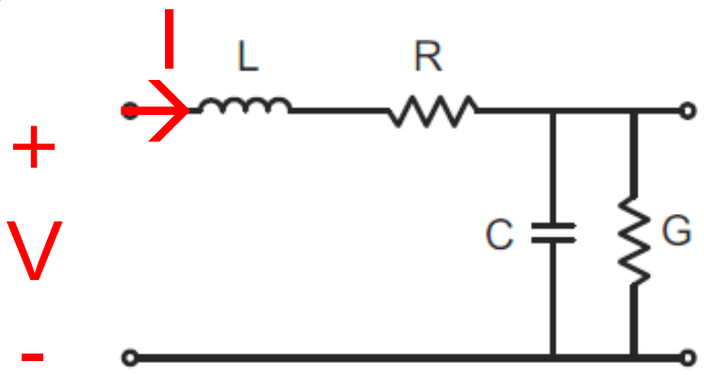




Model Everything

T-line Theory & Testbench

Theory



$$\frac{\partial V(x)}{\partial x} = -(R + j\omega L)I(x)$$

$$\frac{\partial I(x)}{\partial x} = -(G + j\omega C)V(x)$$

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$$

$$Z_c = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Testbench

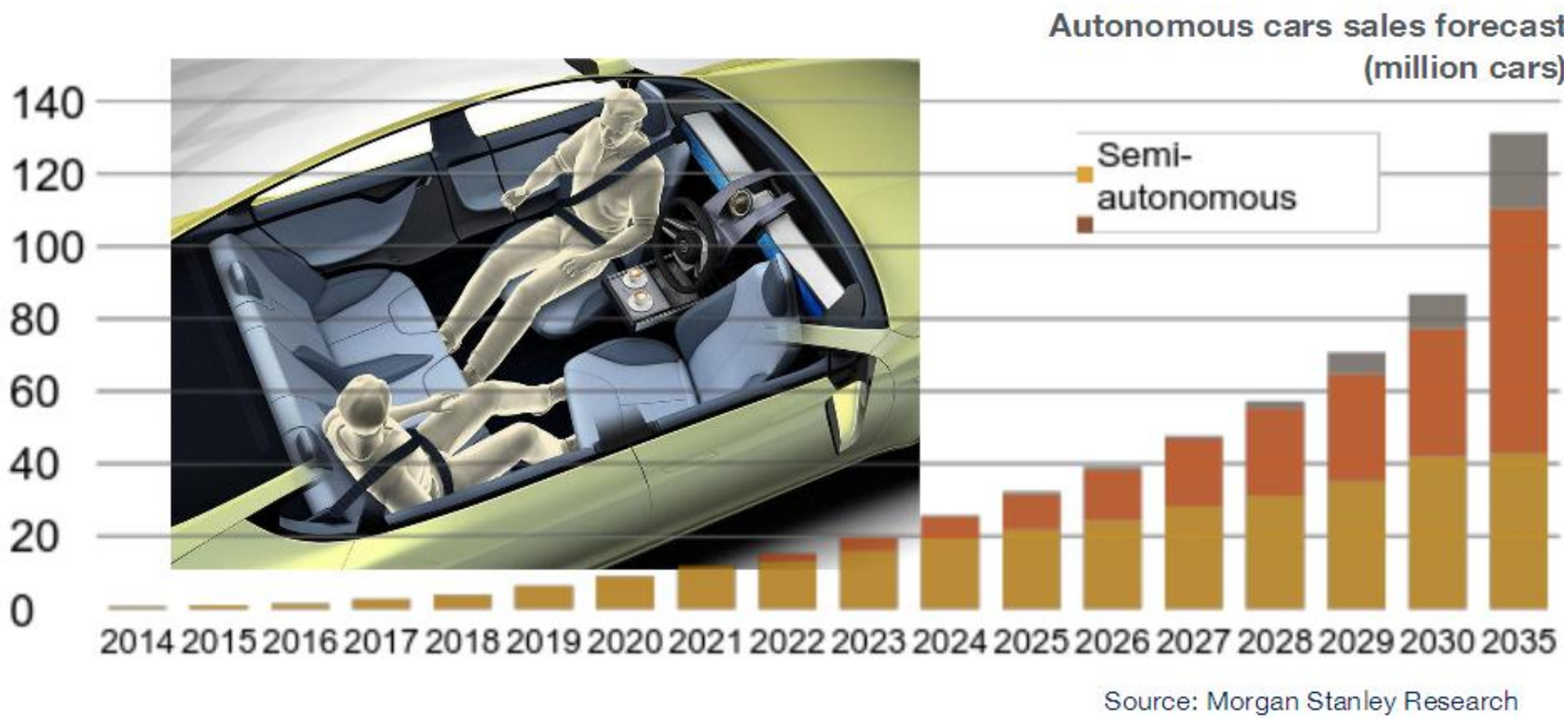
T-line metrics calculated from ABCD parameters

$$Z_c = \sqrt{\frac{B}{C}}$$

$$\alpha = 8.6859 \cdot \Re(cosh^{-1}(A))$$

$$\beta = (180/\pi) \cdot \Im(cosh^{-1}(A))$$

Driverless needs mm-wave nm CMOS



- Every car will be equipped with 10-20 radars to move on its own