

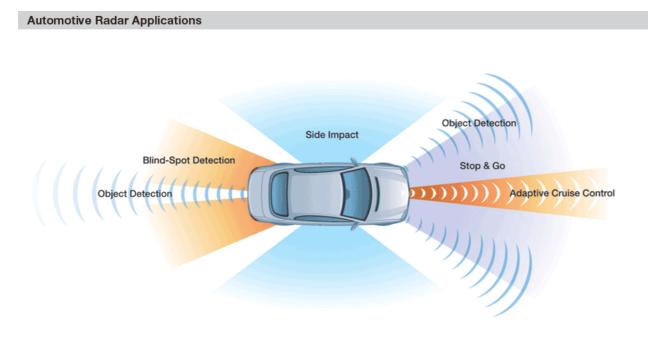
# nm CMOS Device Synthesis for mm-Wave Design

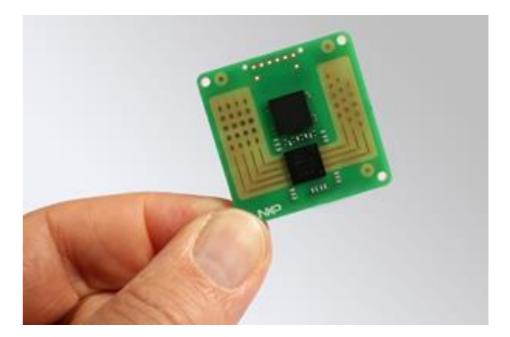
Errikos Lourandakis CDNLive Munich, May 2-4 2016

# Why mm-wave silicon design?

#### m CMOS mm-wave device synthesis

Automotive radar 77-81GHz





Source: NXP, CES 2016

- Long range and short range radar around vehicle for advanced driver assistance systems (ADAS)
- Existing solutions in SiGe and now CMOS
- Demand for ADAS is massive ~ Millions of units/year



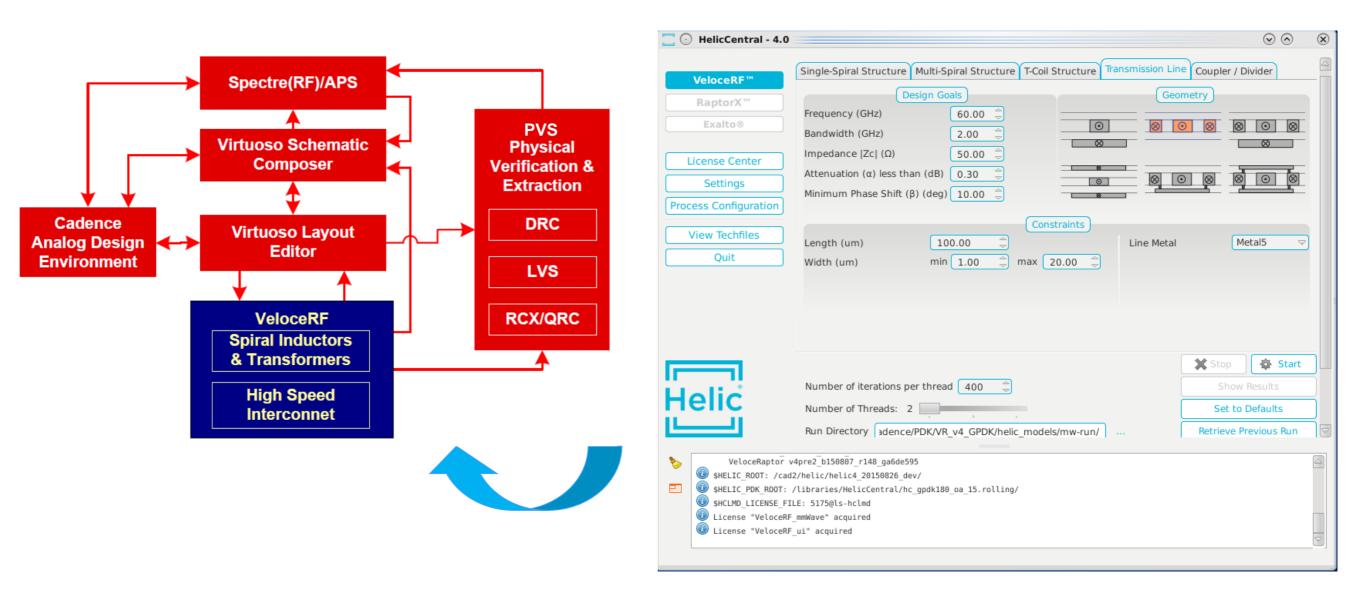
## mm-wave silicon with Helic

Helic's PCell synthesis inside Cadence Virtuoso

- > mm-wave Transmission Lines, Bends, Junctions
- >> mm-wave Couplers
- > DRC, LVS clean SKILL PCells
- Schematic and layout views for Cadence PVS flow
- RLCk and S-par models suitable for frequency and time domain analyses within Virtuoso ADE
- PCell synthesis down to 7nm/10nm/16nm CMOS



# Where does Helic come into play?



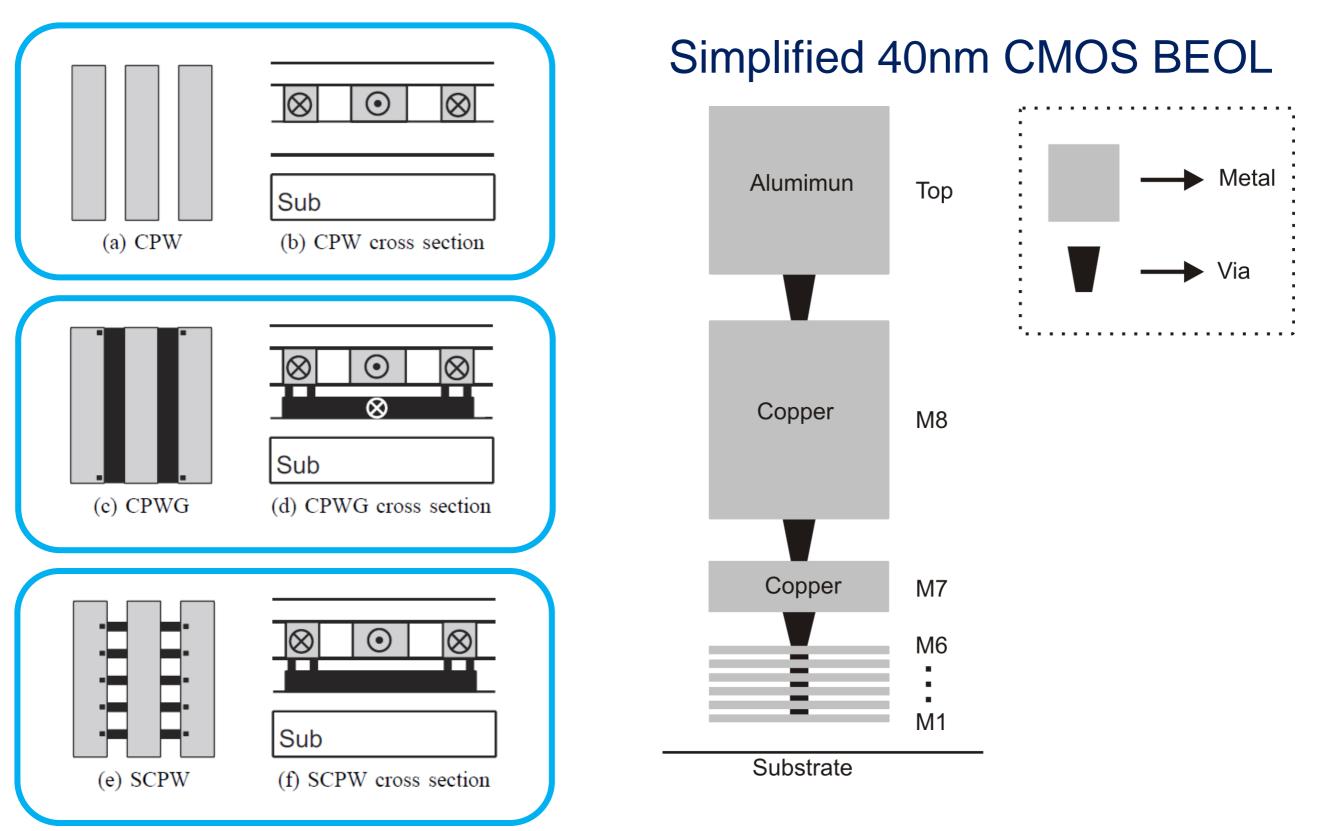
mm-wave device synthesis integrated in Cadence
 Transmission lines, bends and couplers
 DRC, LVS clean PCells ready for mm-wave design

# mm-wave Device Synthesis

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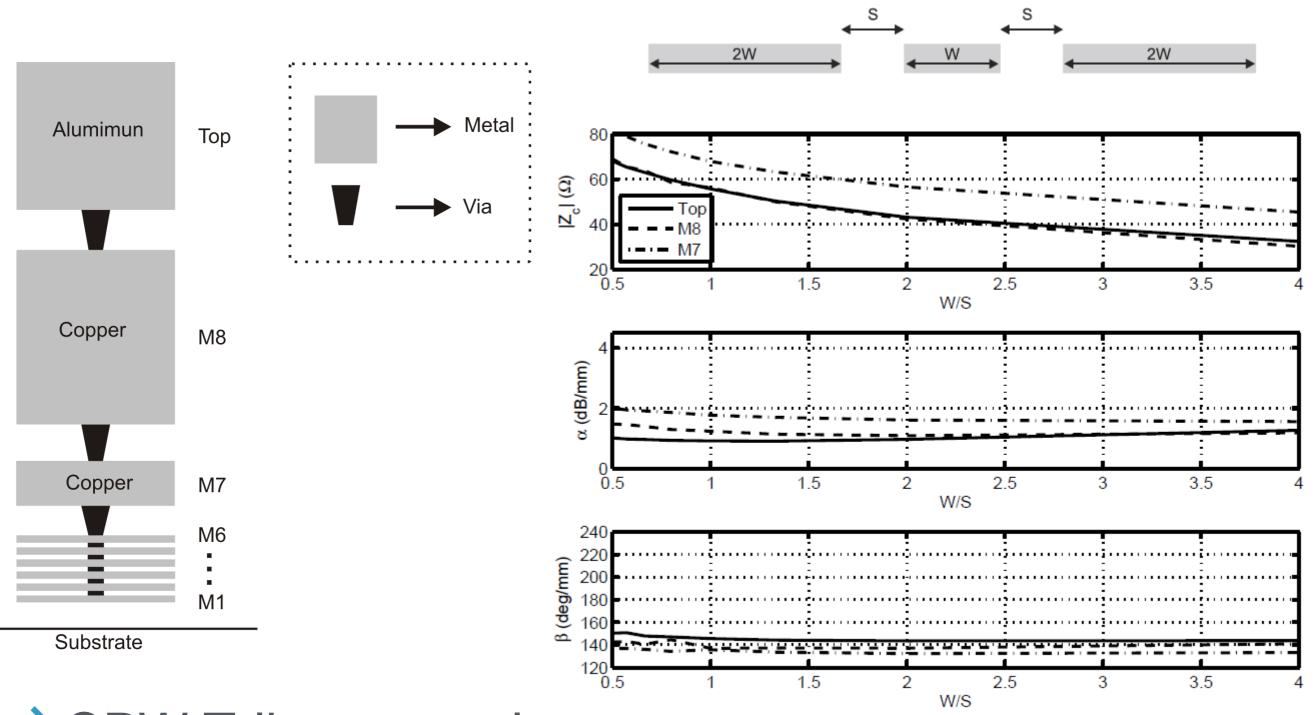
- U License "VeloceRF\_mmWave" acquired
- License "VeloceRF\_ui" acquired

# **CMOS Transmission Lines**





# Where is the challenge?



# CPW T-line example Parametric analysis @ 60GHz

## mm-wave T-line Synthesis

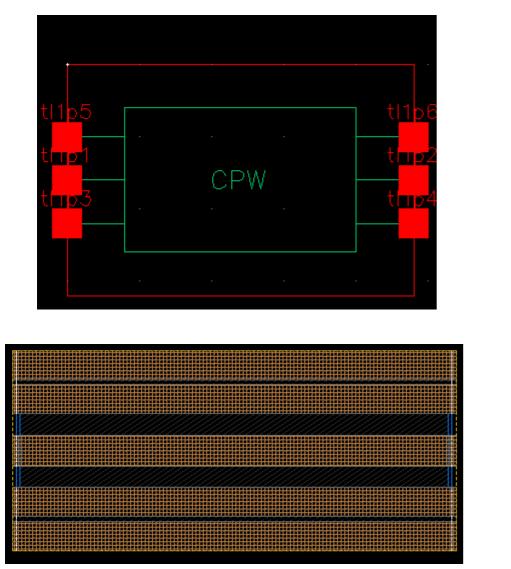
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	<ul> <li>Solution</li> <li>Playe</li> <li>Remove</li> </ul>	<b>F (GHz)</b> 50	<b>Zc (Ohm)</b> 50.0748	<b>Z Low (Ohm)</b> 50.0513	50.0985	Attenuation (dB) 0.258434	Phase Shift (deg) 29.251	Length (um) 250	Width (um 11.6			
	O Solution	<b>F (GHz)</b> 50 50	<b>Zc (Ohm)</b> 50.0748 50.0351	Z Low (Ohm) 50.0513 49.9971	50.0985 50.0732	Attenuation (dB) 0.258434 0.288849	Phase Shift (deg) 29.251 29.2078	Length (um) 250 250	Width (um 11.6 17.8	_		
	<ul> <li>Solution</li> <li>Playe</li> <li>Remove</li> </ul>	<b>F (GHz)</b> 50 50 50	<b>Zc (Ohm)</b> 50.0748 50.0351 50.0558	Z Low (Ohm) 50.0513 49.9971 50.0302	50.0985 50.0732 50.0814	Attenuation (dB) 0.258434 0.288849 0.262721	Phase Shift (deg) 29.251 29.2078 29.3584	Length (um) 250 250 250 250	Width (um 11.6 17.8 12.4			
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VeloceR WeloceR SHELIC_ROOT SHELIC_POK SHELIC_POK SHELIC_POK SHELIC_POK SHELIC_POK SHELIC_POK SHELIC_POK	<ul> <li>Solution</li> <li>Playe</li> <li>Remove</li> </ul>	<b>F (GHz)</b> 50 50 50 50 50 50	<b>Zc (Ohm)</b> 50.0748 <b>50.0351</b> 50.0558 50.0141 49.9897	<b>Z Low (Ohm)</b> 50.0513 <b>49.9971</b> 50.0302 49.9847 49.9576	50.0985 50.0732 50.0814 50.0435 50.0219	Attenuation (dB) 0.258434 0.288849 0.262721 0.267343 0.273979	Phase Shift (deg) 29.251 29.2078 29.3584 28.7718 28.9144	Length (um) 250 250 250 250 250 250	Width (um 11.6 17.8 12.4 14 15.2 18			

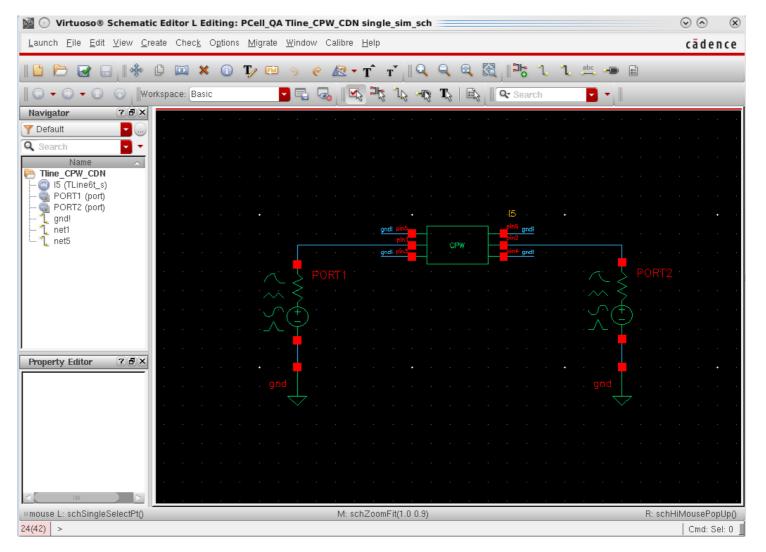
Synthesis returns multiple solutions matching user defined constraints

Layout, schematic, and symbol views including RLCk model at your finger tips



# **Registered DFII views**





 Automatically generated testbench
 Device model suitable for frequency and time domain analyses in ADE

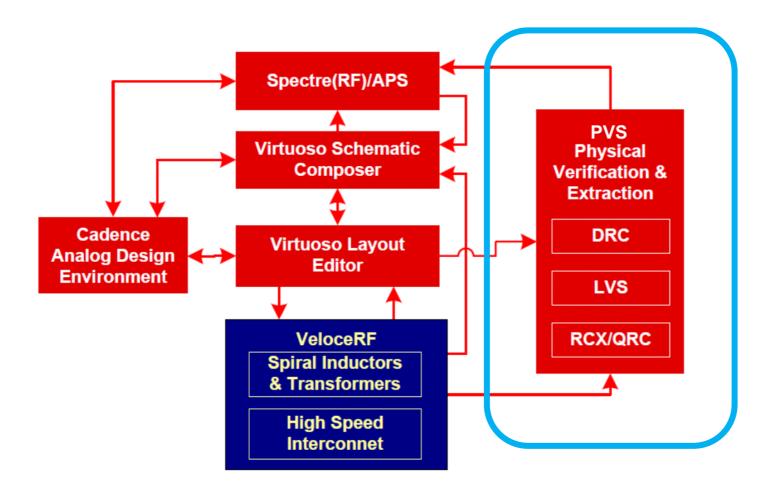


# PCell verification using Spectre

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49		freq (GHz)	12010



# Integration to Physical Verification



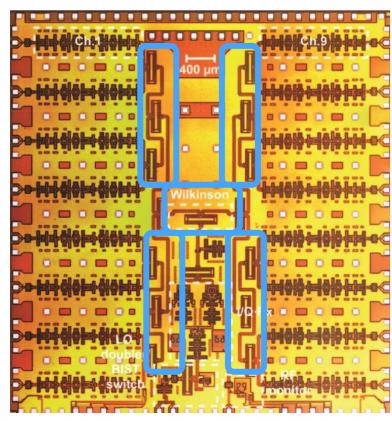
PCell inserted in top-level layout

User runs PVS DRC, LVS as usual in top-level layout

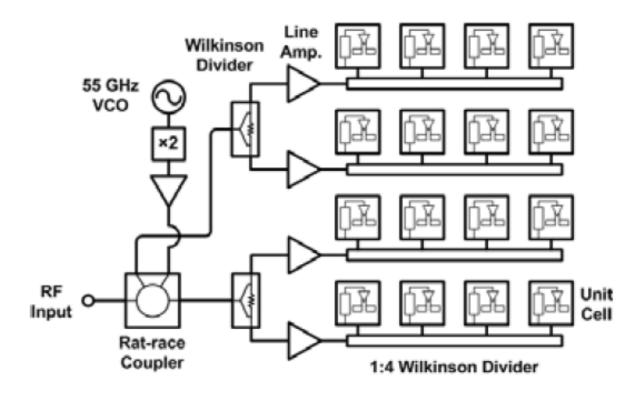
Quantus QRC invoked from layout for extracting parasitic components of entire circuit



## Are mm-wave passives relevant?



Source: UC San Diego, IEEE 2015 Multi-channel 77-81GHz SiGe radar



Source: UC San Diego, IEEE 2015 110 GHz Transmit Phased Array Topology

 T-lines and mm-wave couplers (e.g. Wilkinson divider) are key building blocks
 Physics for nm CMOS design are complex
 Automated and constraint driven design is needed



# Helic's unique mm-wave flow

#### Example 1

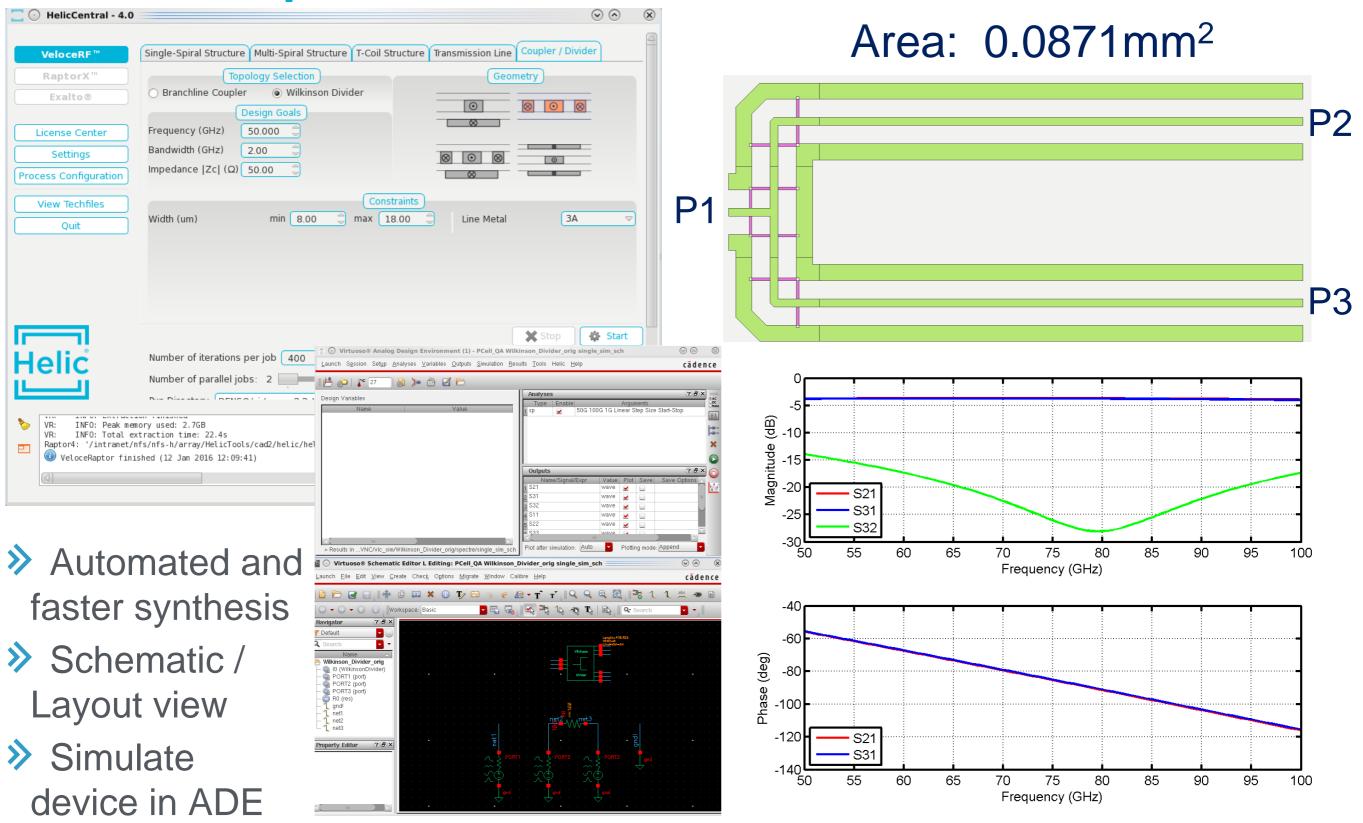
- Synthesis of Wilkinson divider by VeloceRF
- 77-81GHz tuned divider
- Fully customizable PCell in Cadence (DRC, LVS, PVS compliant)

#### Example 2

- Custom Wilkinson divider design based on Helic's mm-wave PCells (T-lines, Bends and Junctions)
- 77-81GHz tuned divider
- Custom device for Cadence verification flow

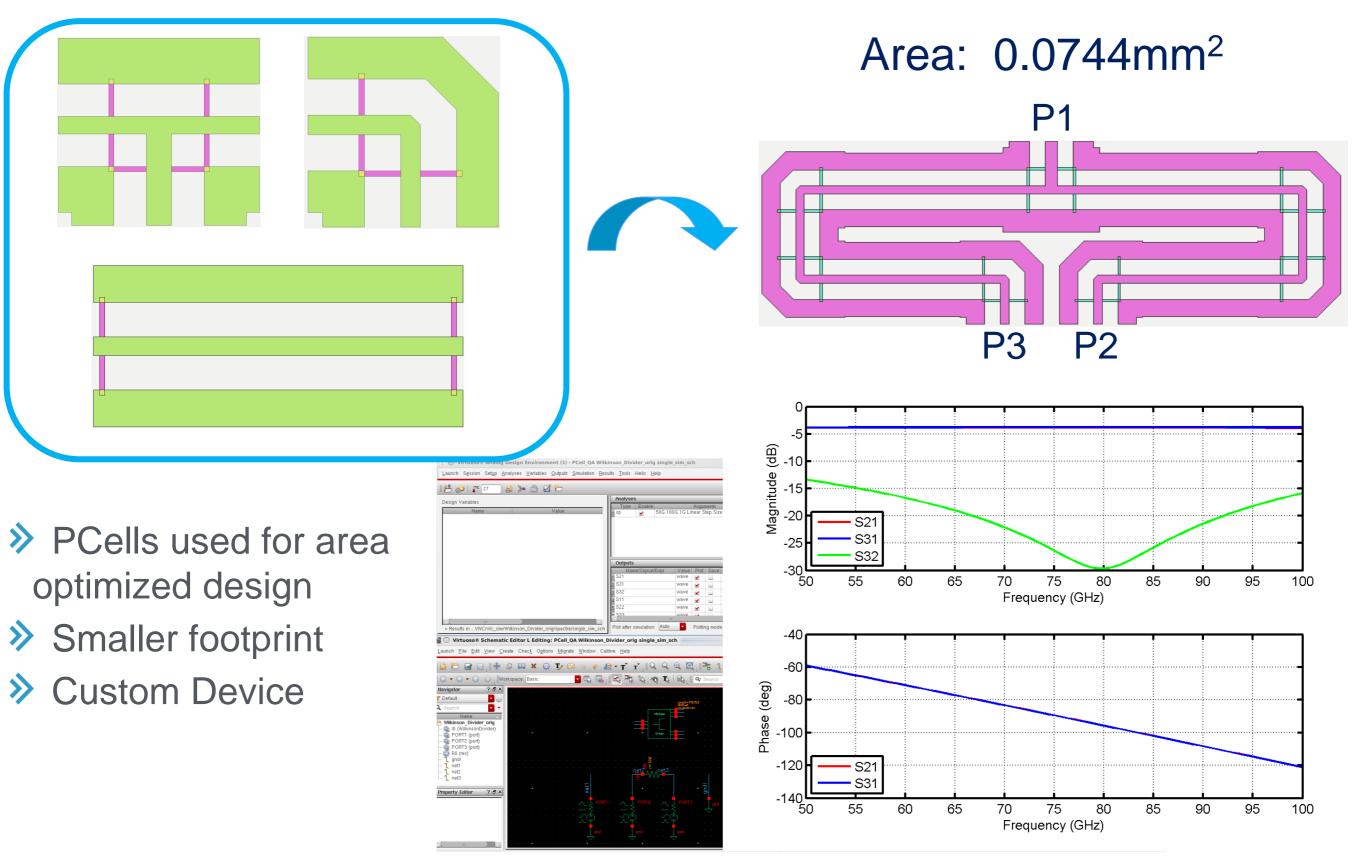


## Example 1 – Divider PCell





## Example 2 – Custom Design

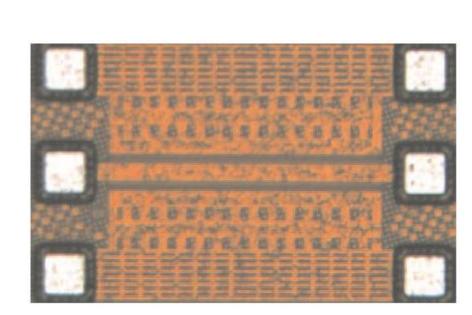


#### mm-wave 40nm CMOS test chip

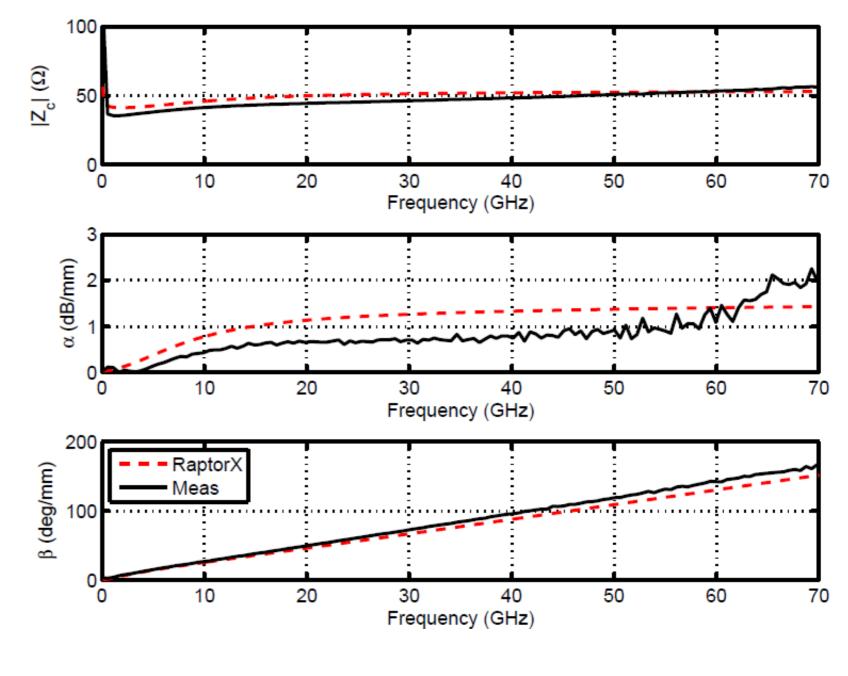
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#### mm-wave Silicon – CPW



CPW T-line



$$Z_{c} = \sqrt{\frac{B}{C}}$$

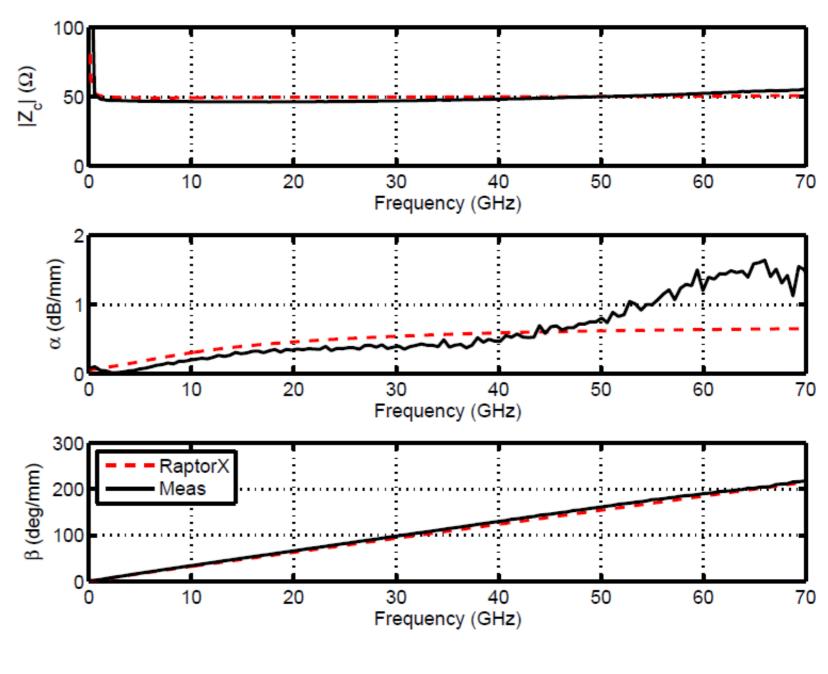
$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A))$$

$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A))$$



#### mm-wave Silicon – SCPW

SCPW T-line



$$Z_c = \sqrt{\frac{B}{C}}$$
  

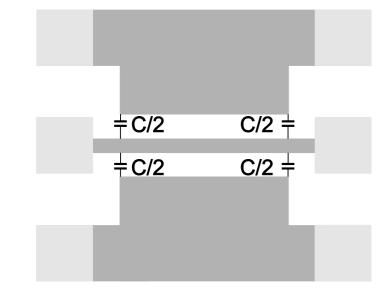
$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A))$$
  

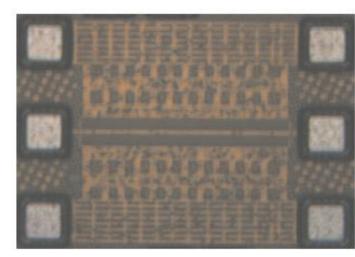
$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A))$$

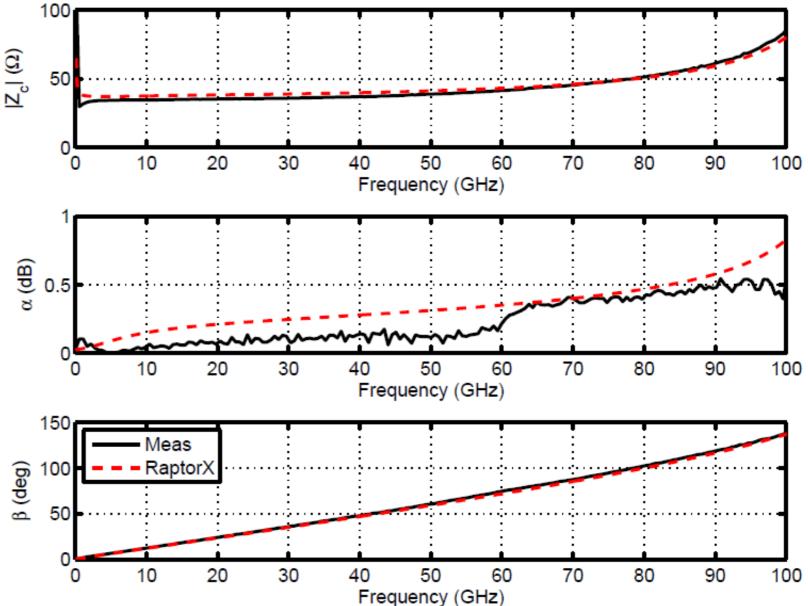


#### mm-wave Silicon – Semi-lumped

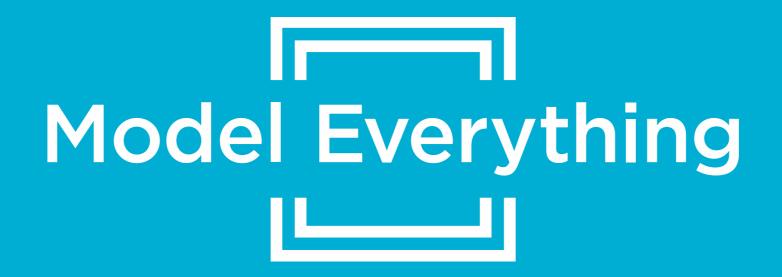




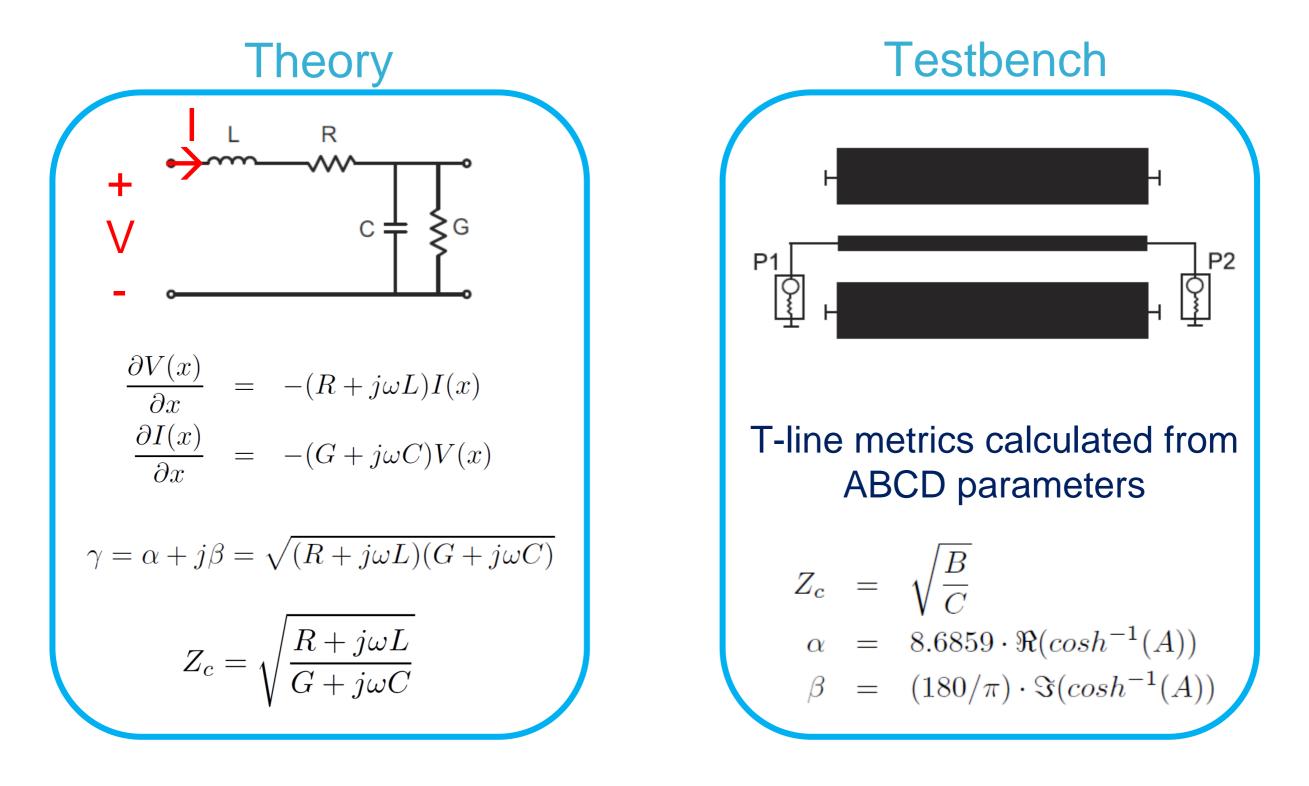






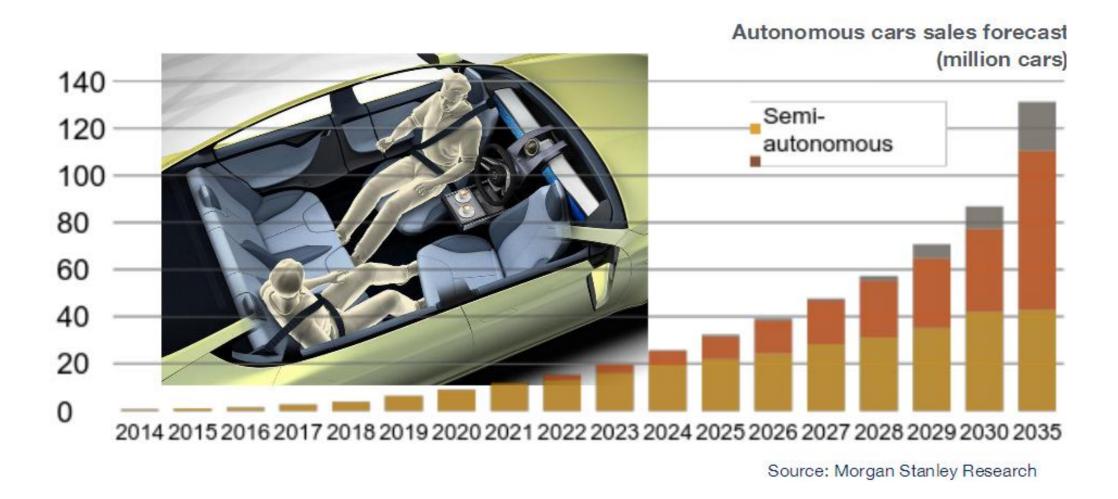


# T-line Theory & Testbench





# Driverless needs mm-wave nm CMOS



# Every car will be equipped with 10-20 radars to move on its own

