Parametric Analysis and Design Guidelines for mm-Wave Transmission Lines in nm CMOS

Errikos Lourandakis, Konstantinos Nikellis, Michail Tsiampas, Shinji Yamaura, Member, IEEE, and Yuu Watanabe

Abstract—This paper focuses on nm CMOS transmission line design as distributed passive elements and their application in mm-wave integrated circuits. A variety of transmission lines such as coplanar waveguides (CPWs), shielded coplanar waveguides (SCPWs), and CPW with ground are analyzed in terms of their geometry and electrical properties. The parametric analysis of the various line types is based on a combination of experimental and simulated data. The slow wave effect of the SCPW is proved to result in better performance, size reduction, and reduced costs compared to the regular CPW. From parametric analysis, a simple set of tests is derived that can easily indicate the capabilities of a certain process design kit in terms of a transmission line design. Finally, in an effort to further reduce silicon area and respective cost, a design technique is proposed with a semilumped CPW transmission line using metal–oxide–metal capacitors as loading elements. This semilumped CPW design achieves nearly double-phase constant per length over the regular CPW and is highly attractive for mm-wave CMOS design.

Index Terms—Millimeter-wave integrated circuits, millimeter-wave measurements, semiconductor device modeling, transmission lines.

I. INTRODUCTION

INTEGRATED circuit design in silicon technologies has undergone an impressive evolution over the last decades. mm-wave CMOS and SiGe design [1] has attracted a lot of attention over the last years, since the availability of silicon technology with transistor cutoff frequencies \( f_T \) in the hundreds of GHz allows for active circuit design in the mm-wave region of 60–110 GHz [2]–[5]. Applications in this mm-wave spectrum include automotive radar systems [6], short-range communications based on IEEE 802.11ad [7], and safety related imaging solutions [8]. The increasing penetration of electronic devices in those new technology sectors has created the opportunity for mass volume consumer markets. The gained momentum for the mm-wave IC design, not solely attributed to the ambitions of the academic community, can be traced back to the major industrial parties who want to cover those mass volume applications. In this context, the focus is on the design and characterization of mm-wave integrated transmission lines, which are core building blocks in many aspects of the circuit design process.

Although the design of transmission lines in general has been frequently studied over the years, the effort has been mainly focused on lines implemented on PCB and various package substrates. However, in a modern CMOS process, the design of transmission lines is a significantly more tedious process. First of all, it must be pointed out that the cost per area unit is significantly higher in CMOS compared with PCB and package transmission lines. Therefore, the reduction of line area is of paramount importance, and obtaining lines with maximum phase shift per length is usually a primary consideration for the CMOS designer. A second challenge in the CMOS design lies with several limitations and constraints that arise from the technology itself. Transmission lines on CMOS are typically fabricated using the upper metals of the back end of line (BEOL) due to their superior conductivity. The BEOL process imposes hard constraints on the size and physical position of those metals, with each layer having specific thickness, conductivity, and height from the silicon substrate. BEOL metals are embedded in silicon oxide dielectrics with relative permittivities typically ranging from 3 to 8. In addition to that, certain design rules limit the minimum and maximum width and minimum spacing of the metal layers, as well as metal density (e.g., dummy fill insertion) in the layout. All these constraints restrain the designer’s flexibility and limit the range of useful transmission lines that can be fabricated on a certain technology. Adding to that, the differences between various technologies make it extremely difficult to migrate designs from one CMOS technology to another, as shown in Fig. 1. The aforementioned limitations require from the designer to obtain at least a rough estimation of the range
of transmission lines than that can be fabricated in a certain technology.

It is evident from the above discussion that a thorough parametric analysis of transmission lines on CMOS will greatly assist the designer in assessing the applicability of a certain CMOS process and the optimum type of transmission lines for a certain design. To the best of our knowledge, relative information in the literature has been rather fragmented in the past something quite expected given the high cost of silicon, which renders multiple tapeouts and relative comparisons extremely expensive. To overcome this impediment, this paper is based on a combination of on-silicon measurements and electromagnetic simulation to present a thorough parametric analysis of transmission lines.

In Section II, the basic types of transmission lines are briefly described. The measurement results from transmission lines fabricated on a test chip in 40-nm CMOS are then presented and they are compared with electromagnetic simulation results for the same devices. Once the accuracy of the simulation results is established, then the data pool can be further augmented using additional electromagnetic simulation data. In Section III follows the parametric investigation of CMOS integrated transmission lines. The device performance is investigated in terms of the transmission line parameters Z, α, and β, with the target to obtain guidelines for the selection of optimum technology process and optimum transmission line type. Finally, in Section IV, a circuit technique for achieving physical size reduction of transmission lines is proposed. A low-pass equivalent network topology that achieves a much smaller physical size [9] is implemented. A reduced size semilumped coplanar waveguide (CPW) design is successfully implemented for the first time in nm CMOS at 80 GHz.

II. TRANSMISSION LINES ON SILICON

Coplanar line geometries are widely adopted in RF and mm-wave IC designs due to several reasons. Coplanar transmission lines are very friendly when it comes to characterization with on-wafer measurements, since the typical RF and mm-wave measurement probes are configured with ground-signal-ground (GSG) probe tips. The symmetrical ground planes in CPW-type transmission lines provide good isolation to surrounding electromagnetic aggressors and at the same time allow for easy shunt connections to ground of other circuit devices. For the CPW of Fig. 2, one can easily identify a central signal propagation path and the symmetrically located coplanar metal segments that provide the current return path. Additionally, the alternating current (ac) signal propagation is influenced by the underlying silicon substrate due to magnetic and electrical coupling. The amount of electromagnetic interaction depends on the substrate resistivity and the conductor’s distance from the silicon substrate. This unwanted electromagnetic interaction between the lossy silicon substrate and the CPW transmission line can be reduced using a CPW with ground (CPWG) transmission line, which has a dedicated metal ground plane that is now part of the current return path. As a result, both the distributed per length inductance $L'$ and capacitance $C'$ of the transmission line are altered, and a shift is expected in the characteristic impedance (see the Appendix). A hybrid solution between the CPW and the CPWG leads to the shielded CPW (SCPW). The SCPW does not have a solid ground plane below the signal path but a grid of metal segments connecting the two coplanar ground paths which acts as a shield. As a consequence, the current return path of the SCPW is similar to the CPW transmission line, since the low impedance path is still on the coplanar ground segments. The perpendicular current flow in the grid segments does not cause magnetic coupling with the signal path; therefore, only an increase in the distributed per length capacitance $C'$ is expected for the SCPW line. The impact on the electrical performance would be a decrease in the characteristic impedance $Z$ and an increase of the phase constant $\beta$ [10]–[12].

For acquiring experimental reference data, CPW, CPWG, and SCPW transmission lines are fabricated on a test chip in 40-nm CMOS. A close look of a typical test structure is shown in Fig. 3. All devices are designed for two-port characterization with a Keysight N5251A vector network analyzer and terminals in GSG configuration with a pitch of 100 $\mu$m. After a successful probe tip calibration [13] on a standard impedance substrate with Cascade infinity probes, S-parameters are obtained for all transmission line devices. L-2L deembedding is applied for removing the pad parasitics [14], and the device metrics of characteristic impedance $Z$, attenuation constant $\alpha$, and phase constant $\beta$ are calculated from the complex propagation constant $\gamma$ [15], [16] (see the Appendix).

The next step of the analysis is to model the exact same devices with an electromagnetic modeling tool. Using Helic’s RaptorX tool, the same metrics as before are calculated. Indicative comparison results between measurement and simulation are shown in Figs. 4 and 5. It can be noticed that the dominant loss factor of CPW and SCPW is different as indicated by the sign of $\Im(Z)$. The imaginary part of $Z$ indicates dielectric loss (positive sign) or conductor loss (negative sign) as the dominant factor and is related to the different
Fig. 4. Measured and simulated device metrics for the 40-nm CMOS CPW transmission line implemented in metal M8 with signal width $W = 18.7 \mu m$ and spacing $S = 10.4 \mu m$.

Fig. 5. Measured and simulated device metrics for the 40-nm CMOS SCPW transmission line, implemented in metal M8 with signal width $W = 8.25 \mu m$, spacing $S = 15.6 \mu m$, and lower shield metal M6.

Fig. 6. Parametric transmission line analysis for a 40-nm BEOL process, signal conductor width $W = 12 \mu m$, and different transmission line types. (a) CPW cross section. (b) CPWG and SCPW cross section. (c) Transmission line metrics at 60 GHz.

As an example, consider the transmission line metrics of Fig. 6, where the CPW transmission line is investigated for different width ($W$) over spacing ($S$) ratios and different BEOL metals of Fig. 1. Changing the width to the spacing ratio of a CPW transmission line largely determines the characteristic impedance $Z$ that governs the ac signal propagation along the device and to a smaller extend the attenuation $\alpha$ and phase constant $\beta$. Changing from one BEOL layer to another affects all metrics at once since the distance to the underlying substrate and metal thickness is altered. Lower thin metals are expected to have higher $L'$, while $C'$ depends on the dielectric constants. By using the per length metrics $\alpha$ (dB/mm) and $\beta$ (degree/mm), a more generic investigation is obtained since these transmission line metrics scale with the device size [18].

It is interesting to investigate the same dependences for the CPWG transmission line, as shown in Fig. 6. Sweeping the $W/S$ ratio again alters the characteristic impedance, but the presence of the additional ground plane below the signal trace dominates the band of achievable values due to the $L'/C'$ ratio (see the Appendix). The lower ground plane interacts, both magnetically and electrically, with the signal trace by changing the per length inductance $L'$ and per length capacitance $C'$. A smaller distance to the lower ground plane decreases the $L'$ due to negative magnetic coupling and increases $C'$ due to reduced spacing.

III. Parametric Analysis

Having established the accuracy of the modeling methodology against measured data, the analysis can be extended to additional devices, using only the electromagnetic modeling results. A large number of transmission lines have been analyzed using simulated data for a variety of technology nodes. The metrics of characteristic impedance $Z$, attenuation constant $\alpha$, and phase constant $\beta$ are calculated for each case, and they are presented in the form of trend plots. In the parametric analysis, a standard 50-\Omega CPW transmission line will serve as the reference design and all other variants shall be compared to that.
In order to improve the device performance of the transmission line and shield it from the underlying silicon substrate, the SCPW layout may be chosen. From the previous theoretical analysis, the SCPW transmission line is expected to yield lower loss and higher phase shift, exactly as manifested by the parametric analysis in Fig. 6. The underlying shield metal does not interact magnetically with the signal trace due to the perpendicular current flows, no $L'$ shift, but has a significant effect on the distributed capacitance $C'$ which increases (lower $Z$, higher $\beta$). Thus, the SCPW has by far the largest phase shift when compared to the CPW and CPWG counterparts on the same metal layer. The CPWG does not have a significant size reduction potential and therefore will be not included in the comparison.

Similar results are obtained when performing the same analysis with different CPW lines as reference. In general, the SCPW transmission line outperforms the regular CPW in terms of loss with the additional advantage of having a higher phase constant due to the slow wave effect. This can be translated into a potential size (and cost) reduction, since a shorter SCPW transmission line can achieve the same electrical length as a CPW and exhibit lower loss. In addition to that, the line is better shielded from the substrate reducing the risk of unwanted coupling. The CPW on the other hand is by far the easiest to design, since the combination of metal layer, signal linewidth, and spacing to the coplanar ground lines determines the characteristic impedance $Z$. In this context, the SCPW is the prime choice for mm-wave CMOS transmission lines.

The parametric analysis can also be used to come up with a methodology for evaluating a semiconductor process in terms of its transmission line performance capabilities. Given that the metal layer of the line is predominantly selected to be one of the thick top layers in order to reduce losses, then the thickness (T) and height from substrate (H) are known. On the other hand, the width (W) is constrained with the limits of $W_{\text{min}}$ and $W_{\text{max}}$ resulting from the minimum allowable and maximum unslotted trace widths, imposed by the design rules (DRC) of the semiconductor process. Similarly, the spacing (S) can be also constrained, with $S_{\text{min}}$ being the minimum allowable metal separation due to DRC. The maximum value $S_{\text{max}}$ is not a hard constraint but corresponds to the designer’s consideration for a coplanar line (after increasing the spacing too much, the line behaves essentially as a microstrip). In this paper, $S_{\text{max}}$ has been selected to be $4 \times W$ for the transmission line cross section of Fig. 6.

The methodology for evaluating a semiconductor process is presented in Table I. By examining proper combinations of $W_{\text{min}}$, $W_{\text{max}}$ and $S_{\text{min}}$, $S_{\text{max}}$ for the thickest metal of a semiconductor process, one can easily calculate the minimum and maximum characteristic impedance that is feasible to be fabricated in this process. For example, simulation of a CPW line of $W_{\text{max}}$ and $S_{\text{min}}$ for the 40-nm process of Fig. 1 yielded a characteristic impedance of 30 $\Omega$ at 60 GHz. All efforts to create a line with smaller impedance than this, both manually and using synthesis tools, were unsuccessful, thus verifying that this is indeed the lower limit for this process. Similar guidelines can also be obtained for the phase shift metric (see Table I). Using these guidelines, a designer can easily evaluate the capabilities of a certain semiconductor process and obtain an estimation of its transmission line range by examining just the three $W, S$ combinations presented in Table I.

IV. REDUCED SIZE TRANSMISSION LINE DESIGN

It has been stated in the previous sections that size reduction and hence the saving of silicon area are of paramount importance in the CMOS transmission line design in order to reduce costs. To this direction, this paper proposes a methodology based on the principle of substituting $\lambda/4$ transmission line segments of initial characteristic impedance $Z$ with equivalent low-pass structures [9]. The resulting new transmission line segments can be made significantly shorter by raising their characteristic impedance level to $\sqrt{2}Z$ and adding shunt capacitors as loading elements, as shown in Fig. 7.

The capacitance value for the equivalent low-pass structure can be calculated by comparing the network parameter $ABCD$ matrix of the quarter-wavelength segment with the corresponding matrix of the low-pass structure, as in [20]

$$C_{\text{eq}} = \frac{1}{\omega \sqrt{2Z}} = \frac{1}{2 \pi f \sqrt{2Z}}.$$  

(1)

In this paper, the CPW transmission line serves as the reference design, and size reduction is attempted. For a characteristic impedance of $Z = 50 \Omega$ and electrical length of 90°, an operating frequency of $f_0 = 78$ GHz is selected. According to the previous analysis and (1), the needed load capacitance $C_{\text{eq}}$ is approximately 29 fF. Silicon-integrated devices of such a small capacitance need careful treatment, and the device models provided by the foundries as part of a process design kit (PDK) may not be accurate enough in the mm-wave frequency range. Therefore, it is of paramount importance to include the capacitors in the layout and model the entire structure in a single extraction, rather than relying on EM models for the transmission line and adding PDK models for the capacitors. In our example, the semilumped CPW transmission line is investigated with different layout options, as shown in Fig. 8. The simplistic approach would be to place...
a shunt capacitor of the desired value at each transmission line terminal, as shown in Fig. 8(a). However, for symmetry purposes, two parallel MOM capacitors are preferably placed as loading elements, as shown in Fig. 8(b), to preserve the characteristics of the ac signal propagation as known from the regular CPW. The improved RF performance of the optimized semilumped device is experimentally verified in Fig. 9.

For verification of the proposed design technique, the transmission line metrics for this reduced size design are calculated, as indicated in Fig. 9. Besides the good agreement between the measured and modeled device metrics, the expected electrical performance of characteristic impedance $Z \approx 50 \, \Omega$ at 78 GHz and phase shift $\beta \approx 99^\circ$ compared to an ideal value of 90°, at the desired frequency range around 78 GHz is verified. The reduced size semilumped CPW design achieves a phase constant $\beta = 290^\circ/\text{mm}$ at 60 GHz, which is almost a 2× improvement compared to the CPW data, and proves the validity of the proposed design technique.

An alternative way to evaluate the designed transmission lines for their size reduction potential is to extract the effective relative dielectric permittivity $\varepsilon_r$ associated with the equivalent RLCG model (see the Appendix). The effective relative dielectric constant $\varepsilon_r$ is directly linked to the guided wavelength $\lambda_g = c_0/(f \sqrt{\varepsilon_r})$ of the ac signal and is given as $\varepsilon_r = c_0^2 \cdot L' \cdot C'$, where $L'$ and $C'$ are the distributed per length inductance and capacitance (see the Appendix), and $c_0$ is the free space light velocity. As can be seen in Fig. 10, the SCPW and semilumped CPW clearly outperform the regular CPW transmission line in terms of size reduction potential. Especially, the semilumped CPW achieves by far the highest $\varepsilon_r$ resulting in the shortest guided wavelength $\lambda_g$ and the highest slow wave factor $\text{SWF} = (\varepsilon_r \text{ (type II) } / \varepsilon_r \text{ (CPW)})^{1/2} = 1.96$ for the same signal metal at 60 GHz. This result is also in good agreement with the measured per length phase constant ratio.

A comparison of various mm-wave transmission line designs is provided in Table II for a variety of semiconductor processes. It is interesting to note the widespread of the device metrics in terms of loss and phase shift, which is another manifestation of how the BEOL cross section, the substrate conductivity, and the electrical metal properties affect the

<table>
<thead>
<tr>
<th>Reference</th>
<th>Transmission Line Type</th>
<th>Semiconductor Process</th>
<th>$Z , @ , 60 , \text{GHz}$*</th>
<th>$\alpha , @ , 60 , \text{GHz}$*</th>
<th>$\beta , @ , 60 , \text{GHz}$*</th>
</tr>
</thead>
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<tr>
<td>[12]</td>
<td>SCPW</td>
<td>65 nm CMOS</td>
<td>$\approx 45 , \Omega$</td>
<td>$\approx 0.65 , \text{dB/mm}$</td>
<td>$\approx 286 , \text{deg/mm}$</td>
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<td>[21]</td>
<td>SCPW</td>
<td>65 nm CMOS</td>
<td>$\approx 35 , \Omega$</td>
<td>$\approx 1.1 , \text{dB/mm}$</td>
<td>-</td>
</tr>
<tr>
<td>[22]</td>
<td>Microstrip Line</td>
<td>90 nm CMOS</td>
<td>$\approx 65 , \Omega$</td>
<td>$\approx 1.1 , \text{dB/mm}$</td>
<td>$\approx 135 , \text{deg/mm}$</td>
</tr>
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<td>[23]</td>
<td>Microstrip Line</td>
<td>0.13 μm SiGe BiCMOS</td>
<td>$\approx 50 , \Omega$</td>
<td>$\approx 0.5 , \text{dB/mm}$</td>
<td>-</td>
</tr>
<tr>
<td>[24]</td>
<td>Shielded Microstrip</td>
<td>0.13 μm CMOS</td>
<td>$\approx 45 , \Omega$</td>
<td>$\approx 1 , \text{dB/mm}$</td>
<td>$\approx 370 , \text{deg/mm}$</td>
</tr>
<tr>
<td>[25]</td>
<td>Microstrip Line</td>
<td>45 nm CMOS</td>
<td>$\approx 45 , \Omega$</td>
<td>$\approx 1 , \text{dB/mm}$</td>
<td>$\approx 140 , \text{deg/mm}$</td>
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<td>[26]</td>
<td>SCPW</td>
<td>High Resistivity 65 nm CMOS</td>
<td>$\approx 65 , \Omega$</td>
<td>$\approx 0.6 , \text{dB/mm}$</td>
<td>-</td>
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<td>[27]</td>
<td>Microstrip Line</td>
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<td>$\approx 50 , \Omega$</td>
<td>$\approx 1.4 , \text{dB/mm}$</td>
<td>$\approx 160 , \text{deg/mm}$</td>
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<td>[28]</td>
<td>CPWG</td>
<td>65 nm CMOS</td>
<td>$\approx 50 , \Omega$</td>
<td>$\approx 0.8 , \text{dB/mm}$</td>
<td>$\approx 143 , \text{deg/mm}$</td>
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<td>[30]</td>
<td>Shielded Microstrip</td>
<td>65 nm CMOS</td>
<td>$\approx 50 , \Omega$</td>
<td>$\approx 0.65 , \text{dB/mm}$</td>
<td>$\approx 126 , \text{deg/mm}$</td>
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<td>[31]</td>
<td>SCPW</td>
<td>28 nm CMOS</td>
<td>$\approx 60 , \Omega$</td>
<td>$\approx 0.8 , \text{dB/mm}$</td>
<td>-</td>
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<td>[32]</td>
<td>SCPW</td>
<td>65 nm CMOS</td>
<td>$\approx 30 , \Omega$</td>
<td>$\approx 1.6 , \text{dB/mm}$</td>
<td>-</td>
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<tr>
<td>This work</td>
<td>CPW</td>
<td>40 nm CMOS</td>
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<td>$1.8 , \text{dB/mm}$</td>
<td>$147 , \text{deg/mm}$</td>
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<td>This work</td>
<td>Semi-Lumped CPW</td>
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<td>$\approx 50 , \Omega , @ , 78 , \text{GHz}$</td>
<td>$1 , \text{dB/mm}$</td>
<td>$290 , \text{deg/mm}$</td>
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*Reference data obtained from figures/tables

Fig. 8. Semilumped CPW transmission line topology and 40-nm CMOS device in metal M8 with signal width $W = 6.5 \, \mu$m, spacing $S = 13.7 \, \mu$m, and device under test length 260 $\mu$m. (a) Semilumped type I. (b) Semilumped type II. (c) Device photograph.

Fig. 9. Comparison of measured and modeled transmission line metrics for reduced size semilumped CPW devices.

Fig. 10. Effective relative dielectric permittivity $\varepsilon_r$ comparison for various mm-wave transmission line designs.

Table II Experimental Data From mm-Wave CMOS Transmission Line Designs
Regardless of the absolute values, the trends observed in this paper for the investigated CMOS designs (CPW, CPWG, and SCPW) are in complete accordance to the previous theoretical analysis and experimental findings from literature. Furthermore, the newly introduced mm-wave semi-lumped CPW design proves to be the most attractive in terms of losses and size reduction.

V. CONCLUSION

A parametric analysis of mm CMOS integrated transmission lines for mm-wave frequencies and appropriate design guidelines is presented in this paper. A variety of coplanar transmission lines such as CPW, CPWG, and SCPW are investigated both in theory and by silicon experiments. An electromagnetic parametric analysis is presented that enables the IC designer to gain understanding of both the transmission line performance and the PDK limits in terms of transmission line design. The analysis demonstrates the slow wave effect of the SCPW line and its suitability for mm-wave designs. Finally, a semilumped CPW design is proposed and successfully implemented on silicon at 80 GHz, proving its superiority in terms of area reduction compared to both CPW and SCPW transmission lines. The proposed semilumped device is highly attractive for mm-wave nm CMOS designs due to its IC area reduction potential and moderate losses.

APPENDIX

From microwave network theory [33], a representation as in Fig. 11 is derived for a generic transmission line of infinitesimal length Δl. The transmission line is a two-wire system with a signal and return path and is described in terms of its distributed inductance L′ (H/m), capacitance C′ (F/m), resistance R′ (Ω/m), and conductance G′ (S/m). The complex propagation constant γ = α + jβ, where α is the attenuation constant and β is the phase constant, is used for describing the ac signal propagation and in its general form (3).

\[
\gamma = \frac{1}{\omega C} \left( \frac{L'}{C'} \right)^{1/2} \]

In case of a lossless transmission line (\(\alpha = 0\)), the characteristic impedance is simplified to

\[
Z = \left( \frac{L'}{C'} \right)^{1/2} \]

Transmission line parameters Z (Ω), α (dB), and β (degree) are derived from an S-parameter testbench, as in Fig. 11(b), and ABCD network parameters are given in the following:

\[
\begin{align*}
\gamma &= \cosh^{-1} \left( \frac{1}{\omega C} \right) \\
Z &= \sqrt{\frac{L}{C}} \\
\alpha &= 8.6859 \cdot \sinh(\gamma) \\
\beta &= 180 \cdot \sinh(\gamma) \\
R' &= \frac{3}{\omega C} \\
L' &= \frac{3}{\omega C} \\
C' &= \frac{3}{\omega C} \\
G' &= \frac{3}{\omega C} \\
\end{align*}
\]

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REFERENCES

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