Parametric Analysis and Design Guidelines for mm-Wave Transmission Lines in nm CMOS

Errikos Lourandakis, Konstantinos Nikellis, Michail Tsiampas, Shinji Yamaura, *Member, IEEE*, and Yuu Watanabe

***Abstract*— This paper focuses on nm CMOS transmission line design as distributed passive elements and their application in mm-wave integrated circuits. A variety of transmission lines such as coplanar waveguides (CPWs), shielded coplanar waveguides (SCPWs), and CPW with ground are analyzed in terms of their geometry and electrical properties. The parametric analysis of the various line types is based on a combination of experimental and simulated data. The slow wave effect of the SCPW is proved to result in better performance, size reduction, and reduced costs compared to the regular CPW. From parametric analysis, a simple set of tests is derived that can easily indicate the capabilities of a certain process design kit in terms of a transmission line design. Finally, in an effort to further reduce silicon area and respective cost, a design technique is proposed with a semilumped CPW transmission line using metal–oxide–metal capacitors as loading elements. This semilumped CPW design achieves nearly double-phase constant per length over the regular CPW and is highly attractive for mm-wave CMOS design.**

***Index Terms*— Millimeter-wave integrated circuits, millimeter-wave measurements, semiconductor device modeling, transmission lines.**

I. Introduction

INTEGRATED circuit design in silicon technologies has undergone an impressive evolution over the last decades. mm-wave CMOS and SiGe design [1] has attracted a lot of attention over the last years, since the availability of silicon technology with transistor cutoff frequencies f_T in the hundreds of GHz allows for active circuit design in the mm-wave region of 60–110 GHz [2]–[5]. Applications in this mm-wave spectrum include automotive radar systems [6], short-range communications based on IEEE 802.11ad [7], and safety related imaging solutions [8]. The increasing penetration of electronic devices in those new technology sectors has created the opportunity for mass volume consumer markets. The gained momentum for the mm-wave IC design, not solely attributed to the ambitions of the academic community, can be traced back to the major industrial parties who want to cover those mass volume applications. In this context, the focus is on the design and characterization of mm-wave integrated transmission lines, which are core building blocks in many aspects of the circuit design process.

Manuscript received January 10, 2018; revised April 25, 2018 and May 23, 2018; accepted May 25, 2018. *(Corresponding author: Errikos Lourandakis.)*

E. Lourandakis, K. Nikellis, and M. Tsiampas are with Helic, Inc. R&D, Santa Clara, CA 95054-1534 USA (e-mail: lourandakis@helic.com).

S. Yamaura is with the Semiconductor Circuit Research Development Division, Denso Corporation, Tokyo 108-0075, Japan.

Y. Watanabe is with Transside LLC, Atsugi 243-0816, Japan.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2018.2846743

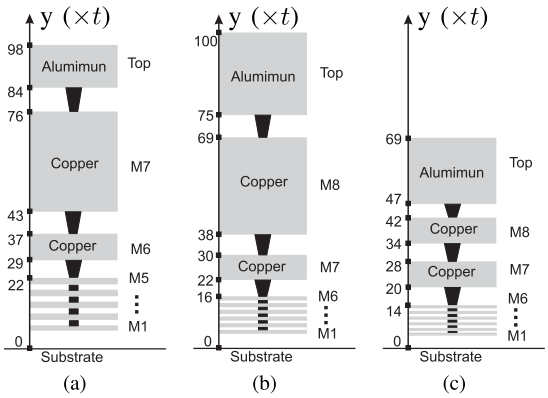

Fig. 1. Simplified cross sections of CMOS BEOL processes with conductor thicknesses and dielectrics in the same y-axis scale. Thickness t of 28-nm BEOL metal M1 is used as y-axis unit. (a) 65-nm BEOL. (b) 40-nm BEOL. (c) 28-nm BEOL.

Although the design of transmission lines in general has been frequently studied over the years, the effort has been mainly focused on lines implemented on PCB and various package substrates. However, in a modern CMOS process, the design of transmission lines is a significantly more tedious process. First of all, it must be pointed out that the cost per area unit is significantly higher in CMOS compared with PCB and package transmission lines. Therefore, the reduction of line area is of paramount importance, and obtaining lines with maximum phase shift per length is usually a primary consideration for the CMOS designer. A second challenge in the CMOS design lies with several limitations and constraints that arise from the technology itself. Transmission lines on CMOS are typically fabricated using the upper metals of the back end of line (BEOL) due to their superior conductivity. The BEOL process imposes hard constraints on the size and physical position of those metals, with each layer having specific thickness, conductivity, and height from the silicon substrate. BEOL metals are embedded in silicon oxide dielectrics with relative permittivities typically ranging from 3 to 8. In addition to that, certain design rules limit the minimum and maximum width and minimum spacing of the metal layers, as well as metal density (e.g., dummy fill insertion) in the layout. All these constraints restrain the designer's flexibility and limit the range of useful transmission lines that can be fabricated on a certain technology. Adding to that, the differences between various technologies make it extremely difficult to migrate designs from one CMOS technology to another, as shown in Fig. 1. The aforementioned limitations require from the designer to obtain at least a rough estimation of the range

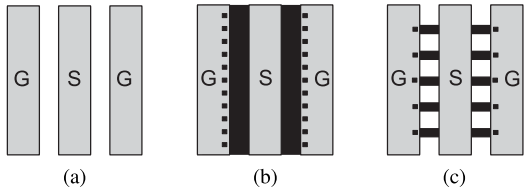

Fig. 2. Example geometries in top view of transmission lines in a simplified CMOS BEOL process. (a) CPW. (b) CPWG. (c) SCPW.

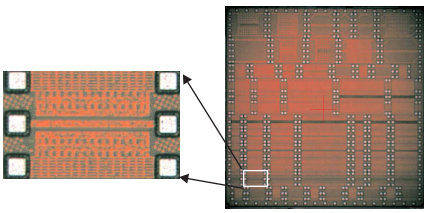

Fig. 3. Transmission line test chip (4 mm × 4 mm) in 40-nm CMOS.

of transmission lines than that can be fabricated in a certain technology.

It is evident from the above discussion that a thorough parametric analysis of transmission lines on CMOS will greatly assist the designer in assessing the applicability of a certain CMOS process and the optimum type of transmission lines for a certain design. To the best of our knowledge, relative information in the literature has been rather fragmented in the past something quite expected given the high cost of silicon, which renders multiple tapeouts and relative comparisons extremely expensive. To overcome this impediment, this paper is based on a combination of on-silicon measurements and electromagnetic simulation to present a thorough parametric analysis of transmission lines.

In Section II, the basic types of transmission lines are briefly described. The measurement results from transmission lines fabricated on a test chip in 40-nm CMOS are then presented and they are compared with electromagnetic simulation results for the same devices. Once the accuracy of the simulation results is established, then the data pool can be further augmented using additional electromagnetic simulation data. In Section III follows the parametric investigation of CMOS integrated transmission lines. The device performance is investigated in terms of the transmission line parameters Z, α, and β, with the target to obtain guidelines for the selection of optimum technology process and optimum transmission line type. Finally, in Section IV, a circuit technique for achieving physical size reduction of transmission lines is proposed. A low-pass equivalent network topology that achieves a much smaller physical size [9] is implemented. A reduced size semilumped coplanar waveguide (CPW) design is successfully implemented for the first time in nm CMOS at 80 GHz.

II. Transmission Lines on Silicon

Coplanar line geometries are widely adopted in RF and mm-wave IC designs due to several reasons. Coplanar transmission lines are very friendly when it comes to characterization with on-wafer measurements, since the typical RF and mm-wave measurement probes are configured with ground-signal-ground (GSG) probe tips. The symmetrical ground planes in CPW-type transmission lines provide good isolation to surrounding electromagnetic aggressors and at the same time allow for easy shunt connections to ground of other circuit devices. For the CPW of Fig. 2, one can easily identify a central signal propagation path and the symmetrically located coplanar metal segments that provide the current return path. Additionally, the alternating current (ac) signal propagation is influenced by the underlying silicon substrate due to magnetic and electrical coupling. The amount of electromagnetic interaction depends on the substrate resistivity and the conductor's distance from the silicon substrate. This unwanted electromagnetic interaction between the lossy silicon substrate and the CPW transmission line can be reduced using a CPW with ground (CPWG) transmission line, which has a dedicated metal ground plane that is now part of the current return path. As a result, both the distributed per length inductance L' and capacitance C' of the transmission line are altered, and a shift is expected in the characteristic impedance (see the Appendix). A hybrid solution between the CPW and the CPWG leads to the shielded CPW (SCPW). The SCPW does not have a solid ground plane below the signal path but a grid of metal segments connecting the two coplanar ground paths which acts as a shield. As a consequence, the current return path of the SCPW is similar to the CPW transmission line, since the low impedance path is still on the coplanar ground segments. The perpendicular current flow in the grid segments does not cause magnetic coupling with the signal path; therefore, only an increase in the distributed per length capacitance C' is expected for the SCPW line. The impact on the electrical performance would be a decrease in the characteristic impedance Z and an increase of the phase constant β [10]–[12].

For acquiring experimental reference data, CPW, CPWG, and SCPW transmission lines are fabricated on a test chip in 40-nm CMOS. A close look of a typical test structure is shown in Fig. 3. All devices are designed for two-port characterization with a Keysight N5251A vector network analyzer and terminals in GSG configuration with a pitch of 100 μm. After a successful probe tip calibration [13] on a standard impedance substrate with Cascade infinity probes, S-parameters are obtained for all transmission line devices. L-2L deembedding is applied for removing the pad parasitics [14], and the device metrics of characteristic impedance Z, attenuation constant α, and phase constant β are calculated from the complex propagation constant γ [15], [16] (see the Appendix).

The next step of the analysis is to model the exact same devices with an electromagnetic modeling tool. Using Helic's RaptorX tool, the same metrics as before are calculated. Indicative comparison results between measurement and simulation are shown in Figs. 4 and 5. It can be noticed that the dominant loss factor of CPW and SCPW is different as indicated by the sign of $\Im(Z)$. The imaginary part of Z indicates dielectric loss (positive sign) or conductor loss (negative sign) as the dominant factor and is related to the different

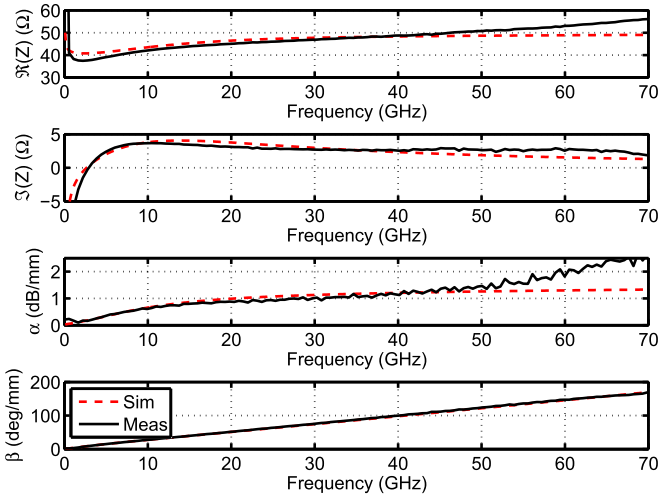

Fig. 4. Measured and simulated device metrics for the 40-nm CMOS CPW transmission line implemented in metal M8 with signal width $W = 18.7$ μm and spacing $S = 10.4$ μm.

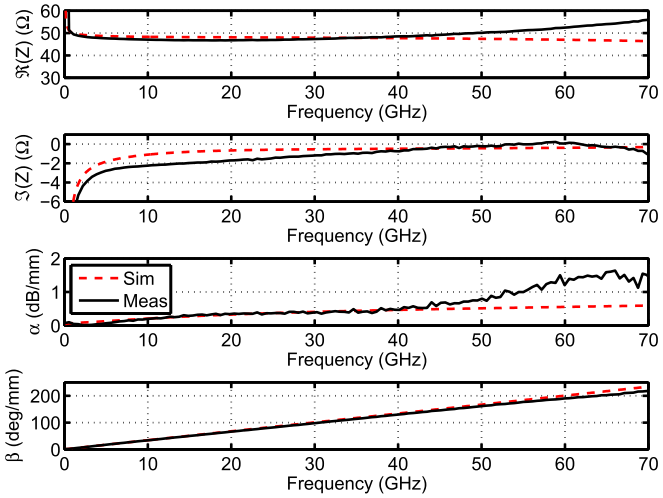

Fig. 5. Measured and simulated device metrics for the 40-nm CMOS SCPW transmission line, implemented in metal M8 with signal width $W = 8.25$ μm, spacing $S = 15.6$ μm, and lower shield metal M6.

current return paths, as discussed earlier. Some deviations in the attenuation constant α and characteristic impedance Z above 60 GHz are most likely due to radiation and multimode propagation in mm-wave on-wafer CPW measurements [17].

III. Parametric Analysis

Having established the accuracy of the modeling methodology against measured data, the analysis can be extended to additional devices, using only the electromagnetic modeling results. A large number of transmission lines have been analyzed using simulated data for a variety of technology nodes. The metrics of characteristic impedance Z, attenuation constant α, and phase constant β are calculated for each case, and they are presented in the form of trend plots. In the parametric analysis, a standard 50-Ω CPW transmission line will serve as the reference design and all other variants shall be compared to that.

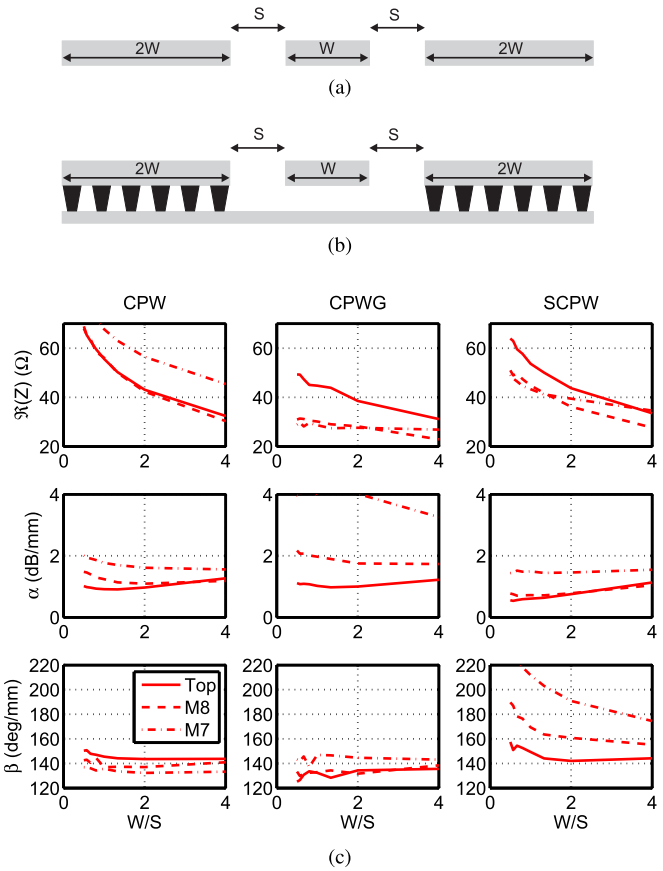

Fig. 6. Parametric transmission line analysis for a 40-nm BEOL process, signal conductor width $W = 12$ μm, and different transmission line types. (a) CPW cross section. (b) CPWG and SCPW cross section. (c) Transmission line metrics at 60 GHz.

As an example, consider the transmission line metrics of Fig. 6, where the CPW transmission line is investigated for different width (W) over spacing (S) ratios and different BEOL metals of Fig. 1. Changing the width to the spacing ratio of a CPW transmission line largely determines the characteristic impedance Z that governs the ac signal propagation along the device and to a smaller extend the attenuation α and phase constant β. Changing from one BEOL layer to another affects all metrics at once since the distance to the underlying substrate and metal thickness is altered. Lower thin metals are expected to have higher L', while C' depends on the dielectric constants. By using the per length metrics α (dB/mm) and β (degree/mm), a more generic investigation is obtained since these transmission line metrics scale with the device size [18].

It is interesting to investigate the same dependences for the CPWG transmission line, as shown in Fig. 6. Sweeping the W/S ratio again alters the characteristic impedance, but the presence of the additional ground plane below the signal trace dominates the band of achievable values due to the L'/C' ratio (see the Appendix). The lower ground plane interacts, both magnetically and electrically, with the signal trace by changing the per length inductance L' and per length capacitance C'. A smaller distance to the lower ground plane decreases the L' due to negative magnetic coupling and increases C' due to reduced spacing.

TABLE I
BEOL METAL PARAMETERS AND TRANSMISSION LINE METRICS

W_{min}, S_{min}	W_{min}, S_{max}	W_{max}, S_{min}	W_{max}, S_{max}
–	MAX Z	MIN Z	–
–	MIN β	–	MAX β

In order to improve the device performance of the transmission line and shield it from the underlying silicon substrate, the SCPW layout may be chosen. From the previous theoretical analysis, the SCPW transmission line is expected to yield lower loss and higher phase shift, exactly as manifested by the parametric analysis in Fig. 6. The underlying shield metal does not interact magnetically with the signal trace due to the perpendicular current flows, no L' shift, but has a significant effect on the distributed capacitance C' which increases (lower Z, higher β). Thus, the SCPW has by far the largest phase shift when compared to the CPW and CPWG counterparts on the same metal layer. The CPWG does not have a significant size reduction potential and therefore will be not included in the comparison.

Similar results are obtained when performing the same analysis with different CPW lines as reference. In general, the SCPW transmission line outperforms the regular CPW in terms of loss with the additional advantage of having a higher phase constant due to the slow wave effect. This can be translated into a potential size (and cost) reduction, since a shorter SCPW transmission line can achieve the same electrical length as a CPW and exhibit lower loss. In addition to that, the line is better shielded from the substrate reducing the risk of unwanted coupling. The CPW on the other hand is by far the easiest to design, since the combination of metal layer, signal linewidth, and spacing to the coplanar ground lines determines the characteristic impedance Z. In this context, the SCPW is the prime choice for mm-wave CMOS transmission lines.

The parametric analysis can also be used to come up with a methodology for evaluating a semiconductor process in terms of its transmission line performance capabilities. Given that the metal layer of the line is predominantly selected to be one of the thick top layers in order to reduce losses, then the thickness (T) and height from substrate (H) are known. On the other hand, the width (W) is constrained with the limits of $W_{\min}$ and $W_{\max}$ resulting from the minimum allowable and maximum unslotted trace widths, imposed by the design rules (DRC) of the semiconductor process. Similarly, the spacing (S) can be also constrained, with $S_{\min}$ being the minimum allowable metal separation due to DRC. The maximum value $S_{\max}$ is not a hard constraint but corresponds to the designer's consideration for a coplanar line (after increasing the spacing too much, the line behaves essentially as a microstrip). In this paper, $S_{\max}$ has been selected to be $4 \times W$ for the transmission line cross section of Fig. 6.

The methodology for evaluating a semiconductor process is presented in Table I. By examining proper combinations of $W_{\min}$, $W_{\max}$ and $S_{\min}$, $S_{\max}$ for the thickest metal of a semiconductor process, one can easily calculate the minimum and maximum characteristic impedance that is feasible to be fabricated in this process. For example, simulation of a CPW line of $W_{\max}$ and $S_{\min}$ for the 40-nm process of Fig. 1 yielded a characteristic impedance of 30 Ω at 60 GHz. All efforts to create a line with smaller impedance than this, both manually and using synthesis tools, were unsuccessful, thus verifying that this is indeed the lower limit for this process. Similar guidelines can also be obtained for the phase shift metric (see Table I). Using these guidelines, a designer can easily evaluate the capabilities of a certain semiconductor process and obtain an estimation of its transmission line range by examining just the three W, S combinations presented in Table I.

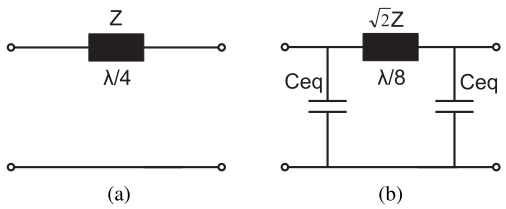

Fig. 7. Two-port network of quarter-wavelength transmission line and its equivalent reduced size low-pass network. (a) $\lambda/4$ transmission line. (b) Reduced size network.

IV. REDUCED SIZE TRANSMISSION LINE DESIGN

It has been stated in the previous sections that size reduction and hence the saving of silicon area are of paramount importance in the CMOS transmission line design in order to reduce costs. To this direction, this paper proposes a methodology based on the principle of substituting $\lambda/4$ transmission line segments of initial characteristic impedance Z with equivalent low-pass structures [9]. The resulting new transmission line segments can be made significantly shorter by raising their characteristic impedance level to $\sqrt{2}Z$ and adding shunt capacitors as loading elements, as shown in Fig. 7.

The capacitance value for the equivalent low-pass structure can be calculated by comparing the network parameter $ABCD$ matrix of the quarter-wavelength segment with the corresponding matrix of the low-pass structure, as in [20]

$$C_{\text{eq}} = \frac{1}{\omega\sqrt{2}Z} = \frac{1}{2\pi f\sqrt{2}Z}. \tag{1}$$

In this paper, the CPW transmission line serves as the reference design, and size reduction is attempted. For a characteristic impedance of $Z = 50$ Ω and electrical length of 90°, an operating frequency of $f_0 = 78$ GHz is selected. According to the previous analysis and (1), the needed load capacitance C_{eq} is approximately 29 fF. Silicon-integrated devices of such a small capacitance need careful treatment, and the device models provided by the foundries as part of a process design kit (PDK) may not be accurate enough in the mm-wave frequency range. Therefore, it is of paramount importance to include the capacitors in the layout and model the entire structure in a single extraction, rather than relying on EM models for the transmission line and adding PDK models for the capacitors. In our example, the semilumped CPW transmission line is investigated with different layout options, as shown in Fig. 8. The simplistic approach would be to place

TABLE II
EXPERIMENTAL DATA FROM mm-WAVE CMOS TRANSMISSION LINE DESIGNS

Reference	Transmission Line Type	Semiconductor Process	Z @ 60 GHz*	α @ 60 GHz*	β @ 60 GHz*
[12]	SCPW	65 nm CMOS	$\approx$ 45 Ω	$\approx$ 0.65 dB/mm	$\approx$ 286 deg/mm
[21]	SCPW	65 nm CMOS	$\approx$ 35 Ω	$\approx$ 1.1 dB/mm	–
[22]	Microstrip Line	90 nm CMOS	$\approx$ 65 Ω	$\approx$ 1.1 dB/mm	$\approx$ 135 deg/mm
[23]	Microstrip Line	0.13 μm SiGe BiCMOS	$\approx$ 50 Ω	$\approx$ 0.5 dB/mm	–
[24]	Shielded Microstrip	0.13 μm CMOS	$\approx$ 45 Ω	$\approx$ 1 dB/mm	$\approx$ 370 deg/mm
[25]	Microstrip Line	45 nm CMOS	$\approx$ 45 Ω	$\approx$ 1 dB/mm	$\approx$ 140 deg/mm
[26]	SCPW	High Resistivity 65 nm CMOS	$\approx$ 65 Ω	$\approx$ 0.6 dB/mm	–
[27]	Microstrip Line	65 nm CMOS	$\approx$ 50 Ω	$\approx$ 1.4 dB/mm	$\approx$ 160 deg/mm
[28]	CPWG	65 nm CMOS	$\approx$ 50 Ω	$\approx$ 0.8 dB/mm	$\approx$ 143 deg/mm
[30]	Shielded Microstip	65 nm CMOS	$\approx$ 50 Ω	$\approx$ 0.65 dB/mm	$\approx$ 126 deg/mm
[31]	SCPW	28 nm CMOS	$\approx$ 60 Ω	$\approx$ 0.8 dB/mm	–
[32]	SCPW	65 nm CMOS	$\approx$ 30 Ω	$\approx$ 1.6 dB/mm	–
This work	CPW	40 nm CMOS	$\approx$ 50 Ω	1.8 dB/mm	147 deg/mm
This work	CPWG	40 nm CMOS	$\approx$ 50 Ω	1.4 dB/mm	134 deg/mm
This work	SCPW	40 nm CMOS	$\approx$ 50 Ω	1.2 dB/mm	190 deg/mm
This work	Semi-Lumped CPW	40 nm CMOS	$\approx$ 50 Ω @ 78 GHz	1 dB/mm	290 deg/mm

*Reference data obtained from figures/tables

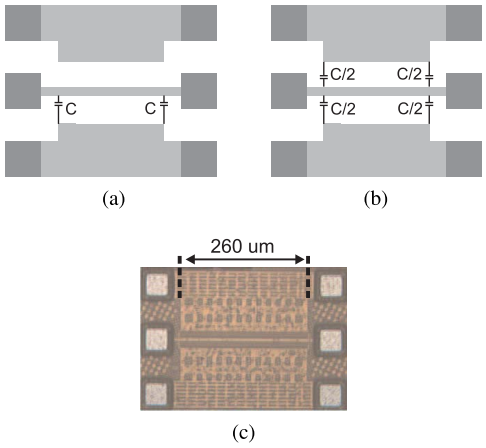

Fig. 8. Semilumped CPW transmission line topology and 40-nm CMOS device in metal M8 with signal width $W = 6.5$ μm, spacing $S = 13.7$ μm, and device under test length 260 μm. (a) Semilumped type I. (b) Semilumped type II. (c) Device photograph.

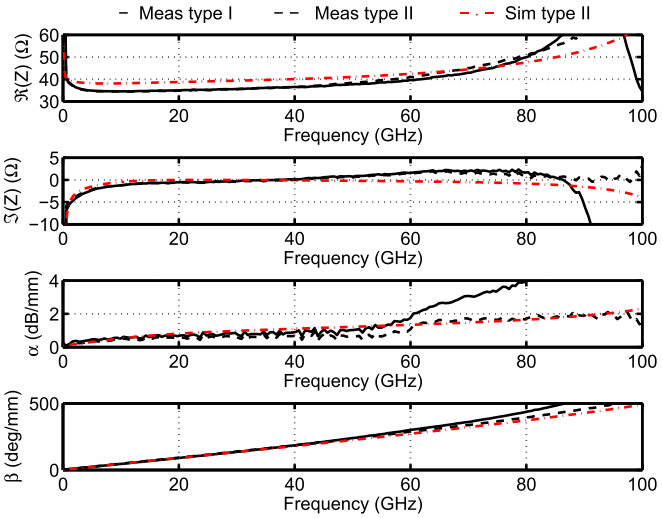

Fig. 9. Comparison of measured and modeled transmission line metrics for reduced size semilumped CPW devices.

a shunt capacitor of the desired value at each transmission line terminal, as shown in Fig. 8(a). However, for symmetry purposes, two parallel MOM capacitors are preferably placed as loading elements, as shown in Fig. 8(b), to preserve the characteristics of the ac signal propagation as known from the regular CPW. The improved RF performance of the optimized semilumped device is experimentally verified in Fig. 9.

For verification of the proposed design technique, the transmission line metrics for this reduced size design are calculated, as indicated in Fig. 9. Besides the good agreement between the measured and modeled device metrics, the expected electrical performance of characteristic impedance $Z \approx 50$ Ω at 78 GHz and phase shift $\beta \approx 99°$, compared to an ideal value of 90°, at the desired frequency range around 78 GHz is verified. The reduced size semilumped CPW design achieves a phase constant $\beta = 290°$/mm at 60 GHz, which is almost a $2\times$ improvement compared to the CPW data, and proves the validity of the proposed design technique.

An alternative way to evaluate the designed transmission lines for their size reduction potential is to extract the effective relative dielectric permittivity ε_r associated with the equivalent RLCG model (see the Appendix). The effective relative dielectric constant ε_r is directly linked to the guided wavelength $\lambda_g = c_0/(f\sqrt{\varepsilon_r})$ of the ac signal and is given as $\varepsilon_r = c_0^2 \cdot L' \cdot C'$, where L' and C' are the distributed per length inductance and capacitance (see the Appendix), and c_0 is the free space light velocity. As can be seen in Fig. 10, the SCPW and semilumped CPW clearly outperform the regular CPW transmission line in terms of size reduction potential. Especially, the semilumped CPW achieves by far the highest ε_r resulting in the shortest guided wavelength λ_g and the highest slow wave factor SWF $= (\varepsilon_r(\text{type II})/\varepsilon_r(\text{CPW}))^{1/2} = 1.96$ for the same signal metal at 60 GHz. This result is also in good agreement with the measured per length phase constant ratio.

A comparison of various mm-wave transmission line designs is provided in Table II for a variety of semiconductor processes. It is interesting to note the widespread of the device metrics in terms of loss and phase shift, which is another manifestation of how the BEOL cross section, the substrate conductivity, and the electrical metal properties affect the

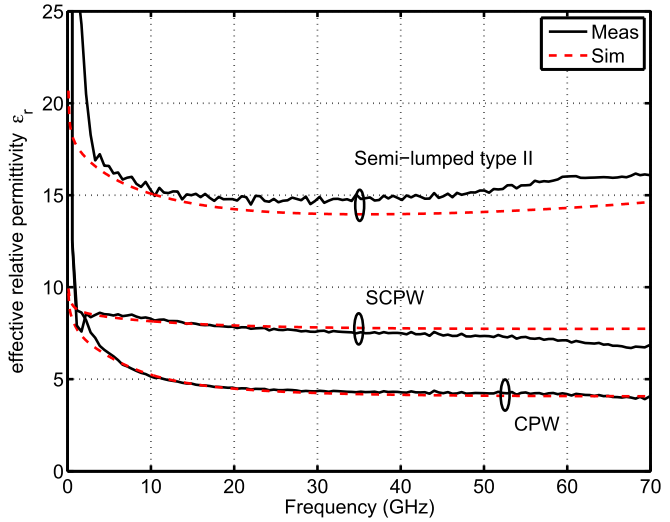

Fig. 10. Measured and simulated effective relative permittivity of investigated 40-nm CMOS transmission lines implemented in metal M8.

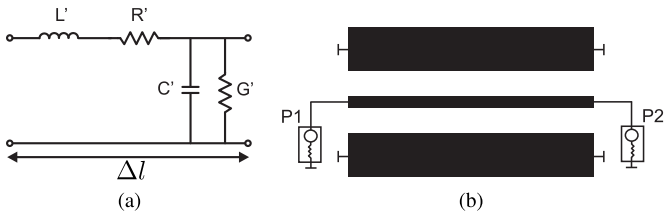

Fig. 11. Equivalent two-port model and transmission line testbench. (a) Equivalent model. (b) Testbench.

transmission line design. Regardless of the absolute values, the trends observed in this paper for the investigated CMOS designs (CPW, CPWG, and SCPW) are in complete accordance to the previous theoretical analysis and experimental findings from literature. Furthermore, the newly introduced mm-wave semi-lumped CPW design proves to be the most attractive in terms of losses and size reduction.

V. Conclusion

A parametric analysis of nm CMOS integrated transmission lines for mm-wave frequencies and appropriate design guidelines is presented in this paper. A variety of coplanar transmission lines such as CPW, CPWG, and SCPW are investigated both in theory and by silicon experiments. An electromagnetic parametric analysis is presented that enables the IC designer to gain understanding of both the transmission line performance and the PDK limits in terms of transmission line design. The analysis demonstrates the slow wave effect of the SCPW line and its suitability for mm-wave designs. Finally, a semilumped CPW design is proposed and successfully implemented on silicon at 80 GHz, proving its superiority in terms of area reduction compared to both CPW and SCPW transmission lines. The proposed semilumped device is highly attractive for mm-wave nm CMOS designs due to its IC area reduction potential and moderate losses.

Appendix

From microwave network theory [33], a representation as in Fig. 11 is derived for a generic transmission line of infinitesimal length Δl. The transmission line is a two-wire system with a signal and return path and is described in terms of its distributed inductance L' (H/m), capacitance C' (F/m), resistance R' (Ω/m), and conductance G' (S/m). The complex propagation constant $\gamma = \alpha + j\beta$, where α is the attenuation constant and β is the phase constant, is used for describing the ac signal propagation and in its general form $\gamma = ((R' + j\omega L')(G' + j\omega C'))^{1/2}$. In case of a lossless transmission line ($\alpha = 0$), the characteristic impedance is simplified to $Z = (L'/C')^{1/2}$ and the phase constant $\beta = \omega\sqrt{L'C'}$. Transmission line parameters Z (Ω), α (dB), and β (degree) are derived from an S-parameter testbench, as in Fig. 11(b), and ABCD network parameters are given in the following:

$$\gamma = \cosh^{-1}(A)/\text{length} \tag{2}$$
$$Z = \sqrt{B/C} \tag{3}$$
$$\alpha = 8.6859 \cdot \Re(\cosh^{-1}(A)) \tag{4}$$
$$\beta = (180/\pi) \cdot \Im(\cosh^{-1}(A)) \tag{5}$$
$$R' = \Re(Z \cdot \gamma) \tag{6}$$
$$L' = \Im(Z \cdot \gamma)/\omega \tag{7}$$
$$C' = \Im(\gamma/Z)/\omega \tag{8}$$
$$G' = \Re(\gamma/Z). \tag{9}$$

Acknowledgment

The authors would like to thank T. Kato and N. Hasegawa of the Denso Corporation for their contribution regarding the experimental on-wafer measurements.

References

[1] F. Dielacher, M. Tiebout, P. Singerl, and D. Seebacher, "Silicon technologies and circuits for RF and mm-wave applications," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol.*, Aug. 2014, pp. 1–5.

[2] K.-L. Wu, K.-T. Lai, R. Hu, C. F. Jou, D.-C. Niu, and Y.-S. Shiao, "77–110 GHz 65-nm CMOS power amplifier design," *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 3, pp. 391–399, May 2014.

[3] A. Medra, V. Giannini, D. Guermandi, and P. Wambacq, "A 79GHz variable gain low-noise amplifier and power amplifier in 28 nm CMOS operating up to 125°C," in *Proc. IEEE 40th Eur. Solid State Circuits Conf.*, Sep. 2014, pp. 183–186.

[4] J. J. Pekarik *et al.*, "A 90nm SiGe BiCMOS technology for mm-wave and high-performance analog applications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Sep./Oct. 2014, pp. 92–95.

[5] G. M. Rebeiz, "Millimeter-wave SiGe RFICs for large-scale phased-arrays," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Sep./Oct. 2014, pp. 56–59.

[6] H. H. Meinel, "Evolving automotive radar—From the very beginnings into the future," in *Proc. IEEE 8th Eur. Conf. Antennas Propag.*, Apr. 2014, pp. 3107–3114.

[7] T. Nitsche, C. Cordeiro, A. B. Flores, E. W. Knightly, E. Perahia, and J. C. Widmer, "IEEE 802.11ad: Directional 60 GHz communication for multi-gigabit-per-second Wi-Fi," *IEEE Commun. Mag.*, vol. 52, no. 12, pp. 132–141, Dec. 2014.

[8] A. M. Niknejad *et al.*, "mm-wave silicon: Smarter, faster, and cheaper communication and imaging," in *Frequency References, Power Management for SoC, and Smart Wireless Interfaces*. Cham, Switzerland: Springer, 2014, pp. 281–295.

[9] T. Hirota, A. Minakawa, and M. Muraguchi, "Reduced-size branch-line and rat-race hybrids for uniplanar MMIC's," *IEEE Trans. Microw. Theory Techn.*, vol. 38, no. 3, pp. 270–275, Mar. 1990.

[10] I. C. H. Lai, H. Tanimoto, and M. Fujishima, "Characterization of high Q transmission line structure for advanced CMOS processes," *IEICE Trans. Electron.*, vol. E89, no. 12, pp. 1872–1879, Dec. 2006.

[11] L. F. Tiemeijer, R. M. T. Pijper, R. J. Havens, and O. Hubert, "Low-Loss patterned ground shield interconnect transmission lines in advanced IC processes," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 3, pp. 561–570, Mar. 2007.

[12] F. Vecchi, M. Repossi, W. Eyssa, P. Arcioni, and F. Svelto, "Design of low-loss transmission lines in scaled CMOS by accurate electromagnetic simulations," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2605–2615, Sep. 2009.

[13] E. Lourandakis, *On-Wafer Microwave Measurements and De-embedding*. Norwood, MA, USA: Artech House, 2016.

[14] H.-T. Yen, T.-J. Yeh, and S. Liu, "A physical de-embedding method for silicon-based device applications," *Online PIERS*, vol. 5, no. 4, pp. 301–305, 2009.

[15] D. F. Williams and R. B. Marks, "Accurate transmission line characterization," *IEEE Microw. Guided Wave Lett.*, vol. 3, no. 8, pp. 247–249, Aug. 1993.

[16] A. M. Mangan, S. P. Voinigescu, M.-T. Yang, and M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 235–241, Feb. 2006.

[17] F. J. Schmückle, R. Doerner, G. N. Phung, W. Heinrich, D. Williams, and U. Arz, "Radiation, multimode propagation, and substrate modes in W-band CPW calibrations," in *Proc. IEEE 41st Eur. Microw. Conf.*, Oct. 2011, pp. 297–300.

[18] L. Ning, K. Matsushita, N. Takayama, K. Okada, and A. Matsuzawa, "Evaluation of a multi-line de-embedding technique up to 110 GHz for millimeter-wave CMOS circuit design," *IEICE Trans. Fundamentals Electron., Commun. Comput. Sci.*, vol. 93, no. 2, pp. 431–439, Feb. 2010.

[19] J. R. Long, Y. Zhao, W. Wu, M. Spirito, L. Vera, and E. Gordon, "Passive circuit technologies for mm-wave wireless systems on silicon," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 8, pp. 1680–1693, Aug. 2012.

[20] E. Lourandakis, M. Schmidt, S. Seitz, and R. Weigel, "Reduced size frequency agile microwave circuits using ferroelectric thin-film varactors," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 3093–3099, Dec. 2008.

[21] M. Varonen, M. Karkkainen, M. Kantanen, and K. A. I. Halonen, "Millimeter-wave integrated circuits in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 1991–2002, Sep. 2008.

[22] J. Brinkhoff, K. Koh, K. Kang, and F. Lin, "Scalable transmission line and inductor models for CMOS millimeter-wave design," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 2954–2962, Dec. 2008.

[23] G. Avenier *et al.*, "0.13μm SiGe BiCMOS technology fully dedicated to mm-wave applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2312–2321, Sep. 2009.

[24] J. J. Lee and C. S. Park, "A slow-wave microstrip line with a high-Q and a high dielectric constant for millimeter-wave CMOS application," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 7, pp. 381–383, Jul. 2010.

[25] T. Quemerais, L. Moquillon, J.-M. Fournier, and P. Benech, "65-, 45-, and 32-nm aluminium and copper transmission-line model at millimeter-wave frequencies," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2426–2433, Sep. 2010.

[26] X.-L. Tang *et al.*, "Performance improvement versus CPW and loss distribution analysis of slow-wave CPW in 65 nm HR-SOI CMOS technology," *IEEE Trans. Electron Devices*, vol. 59, no. 5, pp. 1279–1285, May 2012.

[27] Y. Tsukui, H. Asada, C. Han, K. Okada, and A. Matsuzawa, "Area reduction of millimeter-wave CMOS amplifier using narrow transmission line," in *Proc. IEEE Asia–Pacific Microw. Conf.*, Dec. 2011, pp. 797–800.

[28] R. Minami, C. Han, K. Matsushita, K. Okada, and A. Matsuzawa, "Effect of transmission line modeling using different de-embedding methods," in *Proc. IEEE 41st Eur. Microw. Conf.*, Oct. 2011, pp. 381–384.

[29] A. L. Franc, E. Pistono, G. Meunier, D. Gloria, and P. Ferrari, "A lossy circuit model based on physical interpretation for integrated shielded slow-wave CMOS coplanar waveguide structures," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 754–763, Feb. 2013.

[30] S. Amakawa *et al.*, "Design of well-behaved low-loss millimetre-wave CMOS transmission lines," in *Proc. IEEE 18th Workshop Signal Power Integr.*, May 2014, pp. 1–4.

[31] A. Bautista, A.-L. Franc, and P. Ferrari, "Accurate parametric electrical model for slow-wave CPW and application to circuits design," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 12, pp. 4225–4235, Dec. 2015.

[32] X.-L. Tang, E. Pistono, P. Ferrari, and J.-M. Fournier, "A millimeter-wave CMOS power amplifier design using high-Q slow-wave transmission lines," *Int. J. RF Microw. Comput.-Aided Eng.*, vol. 26, no. 2, pp. 99–109, 2016.

[33] D. M. Pozar, *Microwave Eng.*, 2nd ed. New York, NY, USA: Wiley, 1998.

Errikos Lourandakis received the Diploma degree in electrical and computer engineering from the University of Patras, Patras, Greece, in 2005, and the Ph.D. degree from the Institute for Electronics Engineering, Erlangen, Germany, in 2009.

In 2005, he joined the Institute for Electronics Engineering, as a Research Assistant. His research in the microwave engineering field was focused on device characterization and design of frequency agile microwave circuits. In 2009, he joined Helic Inc., Santa Clara, CA, USA, where he is currently a Senior Research and Development Engineer. He is involved in IC device modeling and physical characterization of integrated devices and mm-wave passives. He authored one book and has authored or co-authored several journal and conference papers.

Konstantinos Nikellis received the Diploma degree in electrical engineering and Ph.D. degree from the National Technical University of Athens (NTUA), Athens, Greece, in 2000 and 2006, respectively.

From 2000 to 2001, he was with the Microwave and Optics Laboratory, NTUA, involved in the design of radar systems for tracking earthquake survivors. In 2001, he joined Helic Inc., Santa Clara, CA, USA, as a Research and Development Engineer involved in the expansion of Helic's EDA tools portfolio, where he has been the Research and Development Director since 2016. He has authored or co-authored several publications in international scientific journals and conferences. His current research interests include design and modeling of RF, mm-wave, and high-speed SoC circuits.

Michail Tsiampas received the Diploma degree in electrical and computer engineering and M.Sc. Diploma degree from the University of Thessaly, Volos, Greece, in 2007 and 2009, respectively, where he is currently pursuing the Ph.D. degree. His prime doctoral research concerns digital timing analysis.

In 2009, he joined Nanotropic S.A., as a core Research and Development Engineer, where he was involved in the development of an industrial EDA tool for simulation and IR-drop analysis in digital designs. Since 2013, he has been a Senior Software Developer with Helic Inc., Santa Clara, CA, USA, where he is involved in the development of parametric cells of inductors and transmission lines.

Shinji Yamaura (M'05) received the B.E. and M.E. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1989 and 1991, respectively.

In 1991, he joined Fujitsu Laboratories Ltd., Kanagawa, Japan, where he was involved in the research and development of simulation modeling, circuit design, and evaluation technology up to 100 GHz for optical communication systems and wireless communication systems such as Mobile-WiMAX and CMOS power amplifiers for WCDMA/LTE. In 2014, he joined the Denso Corporation, Tokyo, where he is currently a Project General Manager with the Semiconductor Circuit Research Development Division. His research and development focuses on the CMOS integrated circuits for a millimeter-wave radar systems.

Mr. Yamaura is a member of the IEEE Solid-State Circuits Society, Microwave Theory and Techniques Society, and IEICE, Japan.

Yuu Watanabe received the B.Sc. and M.E. degrees from Kyoto University, Kyoto, Japan, in 1980 and 1982, respectively, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1997.

In 1982, he joined Fujitsu Ltd., Kanagawa, Japan, where he was involved with the development of high-speed circuits and devices for heterostructure compound semiconductors, including HEMTs, HBTs, and RTDs, and then was involved with CMOS analog and RF circuits. From 2013 to 2016, he was with the Denso Corporation, Tokyo, Japan, where he developed CMOS millimeter-wave integrated circuits. He is currently with Transside LLC, Atsugi, Japan. He is also a Guest Professor with Waseda University, Tokyo.

Dr. Watanabe has served as a member of committee for several academic organizations and conferences, including the International Solid-State Circuits Conference, the International Electron Devices Meeting, VLSI Symposium, the IEICE, Japan, and the IEEE EDS Japan Chapter.